Data Conversion Techniques (DAT115)

Hand-in Report

Second Order Sigma-Delta Modulator
with Interleaving Scheme

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Contents

1. Task Description

The task is to design an ADC which fulfils the following requirements:

- SNDR > 70 dB
- SFDR > 64 dB a
- Band of interest 0 < f < 500 KHz.

In addition to these, area and power estimates should be given. The converter should be described to some detail (including for example resolutions and component values). Specifications should be provided for the necessary filters. AMS 0.35 process will be used for designing the circuitry.

Delimitations

Actual filter design is not necessary, just the specifications.

2. Choosing Converter Type/Our solution

To reach our solution, we have used an iterative process consisting of three major steps: Sigma/delta, second order sigma/delta and interleaved second order sigma/delta. This was done to fulfil the design requirements.

2.a First Order Sigma/Delta

Our first design was a first order sigma/delta converter. This was chosen because of it's good tolerances and relatively low area requirements.

In the ideal case a first order sigma/delta gains 9.03 dB of SNR per doubling of OSR:

$$SNR_{\Sigma\Delta,1} = \frac{12}{8} \cdot k^2 \cdot \frac{3}{\pi^2} \cdot OSR^3$$

Above equation shows that to fulfil our goals we have to use an OSR of 2^8, or 256 times. With the minimum necessary sampling frequency of 1 MHz due to Nyquist limit, this leads to an actual sampling frequency of 256 MHz.

Rough simulations with Simulink have shown that an even higher OSR was needed to fulfil the goals even though simulations are done with a less than complete set of degrading influences. This quickly leads to an operating frequency much too high to cope with the given technology where each op-amp has a settling time of 7ns.

2.b Second Order Sigma/Delta

To improve performance another stage was added to the sigma/delta converter, making it a second-order.

$$SNR_{\Sigma\Delta_2} = \frac{12}{8} \cdot k^2 \cdot \frac{5}{\pi^4} \cdot OSR^5$$

This improves the SNR to 15 dB per OSR doubling in theory. The needed OSR will then be 2^5 in the ideal case.This was shown to be a viable option since the OSR could be reduced to 2^5. However Simulink simulations have shown that with the non-idealities and worst case input the required oversampling rate was 2^7.

In a Sigma/Delta modulator with switch capacitor circuits there will be a minimum of 2 op-amps and a comparator. This gives a delay of 7ns+7ns+0.3ns = 14.3ns. When the oversampling rate is 2^7, the circuit samples at 128MHz (Nyquist limit x OSR) which gives a clock period of 7.81ns. Thus at least the oversampling rate should be reduced to 2^6 which gives a clock period of 15.62ns, yet that is still very close to circuit delay which is 14.3ns.

Possible solutions included pipelinening, yet instead of delving into timing schemes to fulfil our targets, a different approach is taken.

2.c Interleaved Second Order Sigma/Delta

If more converters are run in parallel but off of every other sample and the result is combined afterwards, an improvement in SNR can be shown. For each doubling of the number of parallel converters the SNR should in theory improve by 3 dB. Using 4 second order Sigma/Delta converters to use 2^5 times oversampling, providing a better margin in speed constraints as the clock period is increased to 31.25ns while keeping the circuit delay approximately same around 14.3ns and more than enough time to complete digital reconstruction circuitry.

3. Filters

In the design four different filters are being used: An anti-aliasing filter at the input, a notch filter to ensure removal of the interferer, a noise shaping filter in each converter and finally a recombination filter.

3.a Anti-aliasing filter

The anti-aliasing filter is an analog second order butterworth filter with a corner frequency of 2 MHz. This frequency was chosen because it is some way off the highest information frequency, which means that the signal band will be less attenuated. The normal concern of aliasing won't occur around 500 kHz in our design since we are oversampling – oversampling means that aliasing occurs around a much higher frequency. A butterworth filter was chosen to keep the spectra as flat as possible.

3.b Notch filter

The notch filter is an analog second order Chebychev-II filter centered at 1 MHz. It was deemed necessary to provide adequate rejection of the interferer – it improves SNDR and SFDR by 1.5 dB.

3.c Noise shaping filter

To remove the shaped noise in the converters, a digital fourth order butterworth filter was used, with a corner frequency of 500 kHz. This will give a maximum of 3 dB attenuation to the passband signal. However, this was deemed necessary to reject as much of the noise as possible. Using a fourth order filter also means that it will be closer to ideal filter.

3.d Recombination filter

The recombination of our interleaved signal causes several high-frequency artifacts, as well as some near signal band artifacts. The spectra of the filtered and unfiltered combined output can be observed in figure 1.

To compensate for this, another fourth order digital butterworth filter is used, again with a corner frequency of 500 kHz. This negates the effects of the recombination nicely.

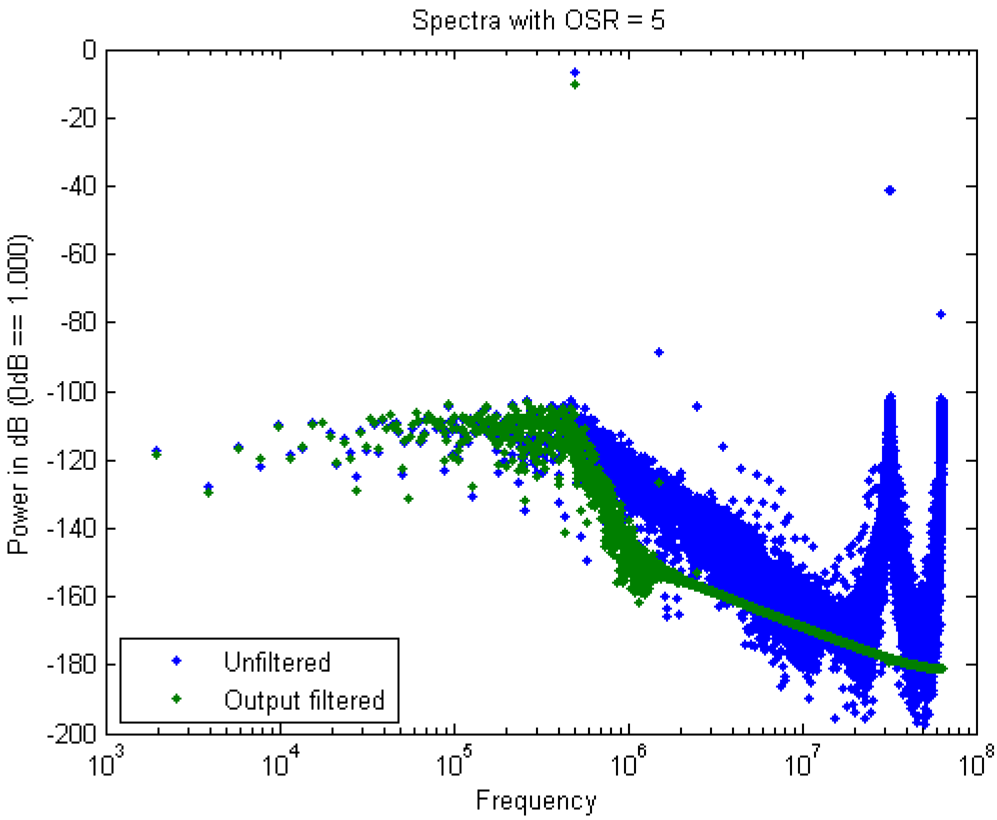

Figure 1: Spectra of the Output Signal (Input Amplitude = 0.9)

4. Simulink Setup

Simulink setup which is controlled by a Matlab file is designed. Constants and design variables are inserted to the m-file which modifies all the values to the correct values in Simulink setup. The Matlab files can be found in appendix.

In the below figure, the overall simulation setup can be observed. Number of scopes and sinks are used for debugging and extracting the simulation results. The interleaving architecture is realized by using two ideal pulses which are made of 4 samples that have a period of ¼ of the desired sampling rate. The two pulses have a phase difference of 180°. Thus within a sample time two raising and two falling edges are created. However it should be noted that these clocks are ideal and do not suffer from jitter.

The combinations of the interleaving arms are done with 4 step counter that has a sampling time ¼ of the system so that data from all four arms can be collected within one sampling time. It should be noted that this switch is also ideal

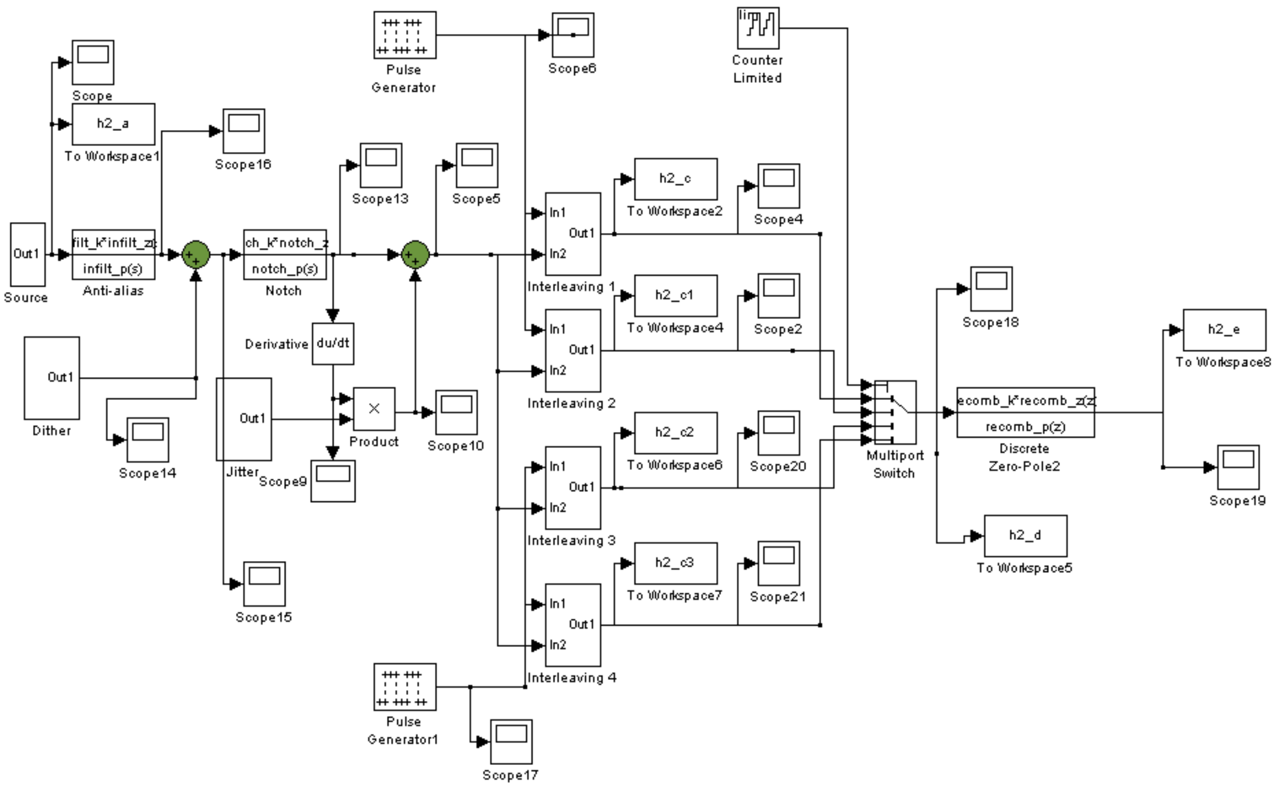

Figure 2: Overall Simulink Setup

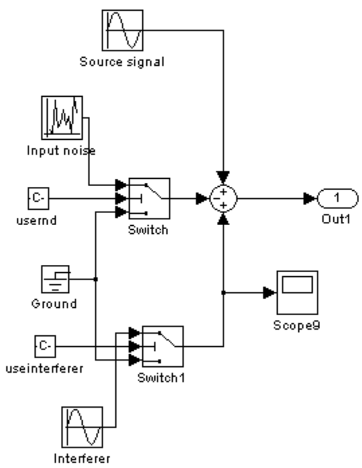

Figure 3: Source Sub-Block

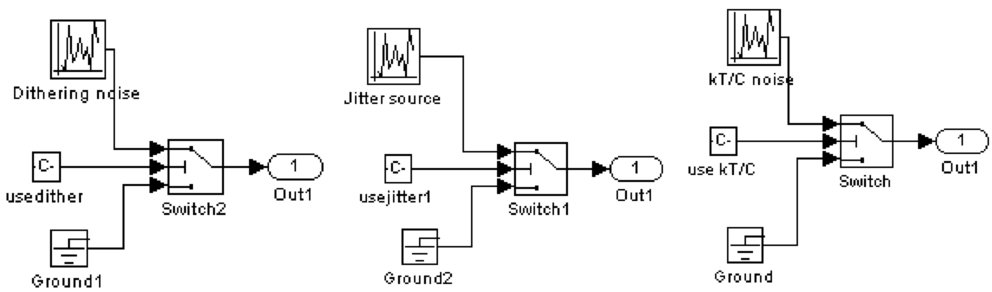

Figure 4: Dither, Jitter and kT/C Sub-Block

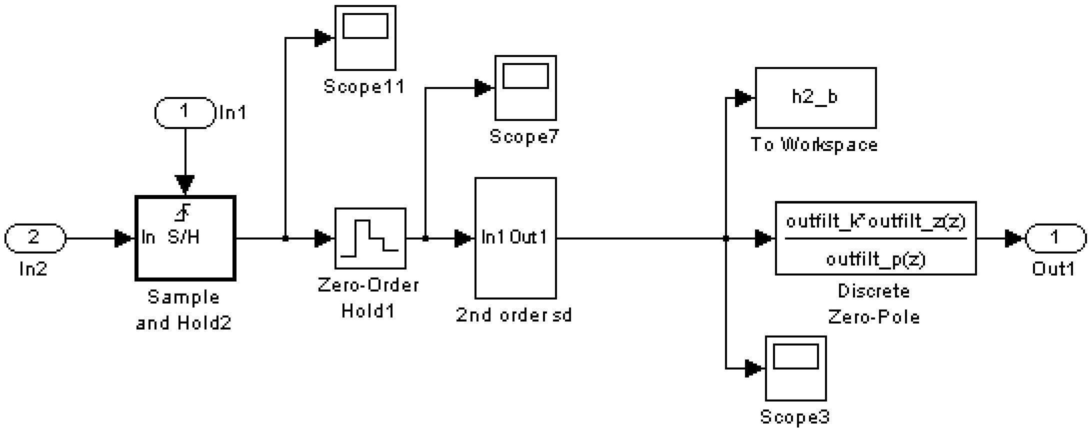

Figure 5: Interleaving Sub-Block

As it can be seen in figure, there are 2 sample&hold circuitries in the design. The first one is used first one is used for implementing the rounding architecture of the interleaving and the second is used for sampling with correct intervals. The filter here is used as the noise shaping filter as described in 3.c.

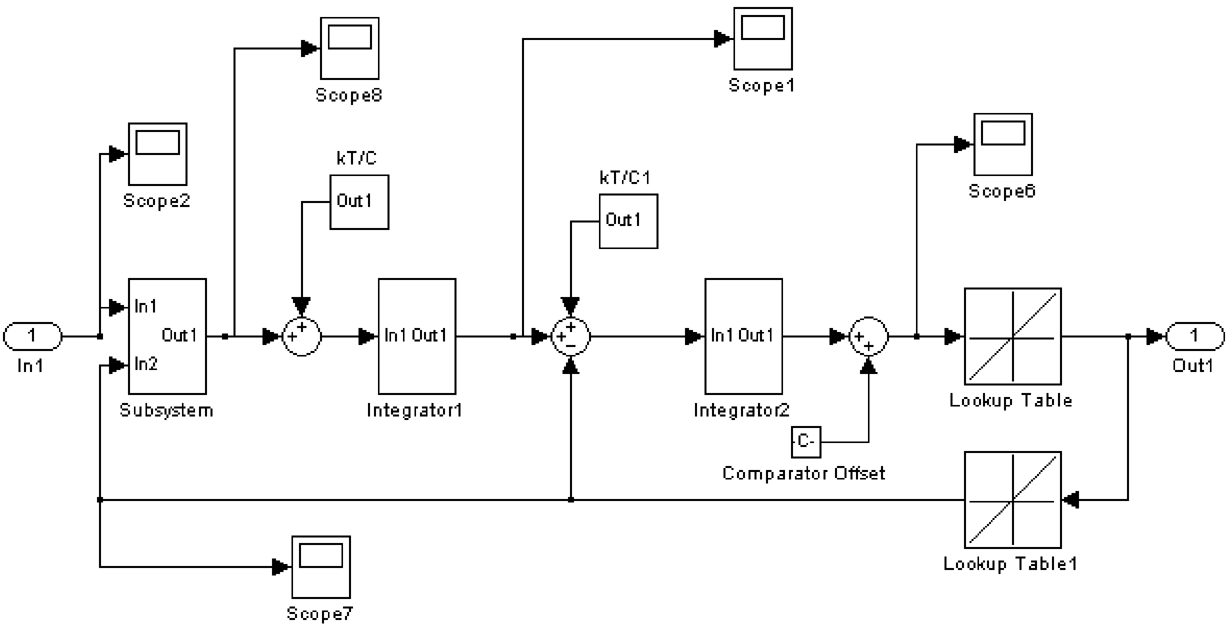

Figure 6: Second Order Sigma/Delta Sub-Block

In circuit wise switched capacitor circuits are planned to be used so that sampling, integration and addition can be implemented with same op-amp within different phases. kT/C noise is added as input referred before the op-amps. 1 bit ADC and DAC are used. Comparator offset is the process dependent offset value in the comparators.

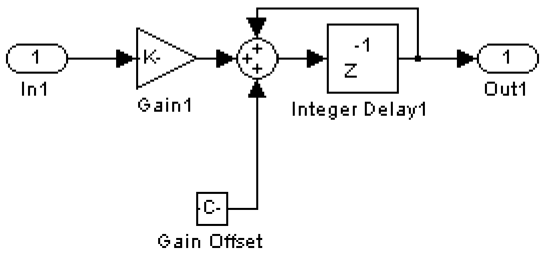

Figure 7: Integrator Sub-Block

While defining the gain, the accuracy of the capacitors and finite open loop gain of the op-amp is used for each block individually. Thus all 8 integrators have different amount of closed loop gain that are around the ideal value of 0.5.

The block gain offset refers to the offset of the op-amps. This process dependent non-ideality when enabled has the ability to make the system suffer up to 40dB of SNR.

5. Simulink Results

5.a MONTE CARLO

Since the introduced non-idealities are random, multiple simulations are necessary to observe their effect correctly. For the system the maximum input amplitude is defined as 0.9, where it is 0.45 in the worst case. The simulations show that the system satisfies the specifications in the worst cases.

The results below are achieved with all the non-idealities except op-amp offset are on with 10 runs. The input amplitude is 0.45:

SNR

OSR	**1**	**2**	**3**	**4**	**5**	**6**
	24.5318	40.5992	54.9335	65.8360	70.5211	73.0125
	24.4731	40.5869	54.6939	65.7670	70.5706	73.0191
	24.5927	40.5890	55.1940	65.7093	70.4673	73.0149
	24.3646	40.5748	55.1931	65.7669	70.5170	73.0028
	24.3967	40.5843	55.2934	65.7852	70.5288	73.0185
	24.4405	40.3010	54.7985	65.9071	70.5521	73.0306
	24.5446	40.4083	54.9620	65.8928	70.5141	73.0041
	24.5233	40.6073	55.1489	65.8914	70.5076	73.0198
	24.6385	40.6284	54.8711	65.7040	70.5092	73.0037
	24.5728	40.6178	54.3924	65.8422	70.5726	73.0150

SNR with Ideal Filter

OSR	**1**	**2**	**3**	**4**	**5**	**6**
	25.9773	41.8199	56.2026	66.2780	70.6787	73.1102
	25.7138	41.8979	55.8229	66.1520	70.7154	73.1194
	26.0377	41.8434	56.4583	66.1817	70.6294	73.1163
	25.8541	41.8473	56.3955	66.2230	70.6641	73.1023
	25.7897	41.8912	56.6171	66.2122	70.6696	73.1175
	25.7990	41.6849	55.9562	66.3690	70.7182	73.1338
	25.9698	41.6018	56.2545	66.3920	70.6771	73.1010
	25.9181	41.8417	56.3329	66.3715	70.6666	73.1221
	26.1093	41.9988	56.0399	66.1848	70.6738	73.1004

25.8576	41.8239	55.5441	66.3223	70.7411	73.1166

SFDR

OSR	1	2	3	4	5	6
	39.8685	54.2002	69.0905	83.3111	87.6825	82.4932
	39.8835	53.6815	68.4476	81.6502	87.3899	82.4930
	41.0310	54.5694	69.7130	81.1601	87.1043	82.4932
	40.7414	54.8125	69.5937	82.5575	87.2504	82.4930
	39.7745	55.0554	70.2331	82.5321	86.7773	82.4926
	40.5548	55.1850	69.7354	82.7084	86.9505	82.4925
	39.8584	55.2289	69.7225	82.6281	87.3584	82.4941
	40.2247	54.5025	69.1691	81.6782	87.2078	82.4932
	40.5985	53.9116	68.6830	82.2701	87.3966	82.4946
	39.7941	53.1246	66.7151	81.2478	87.2637	82.4936

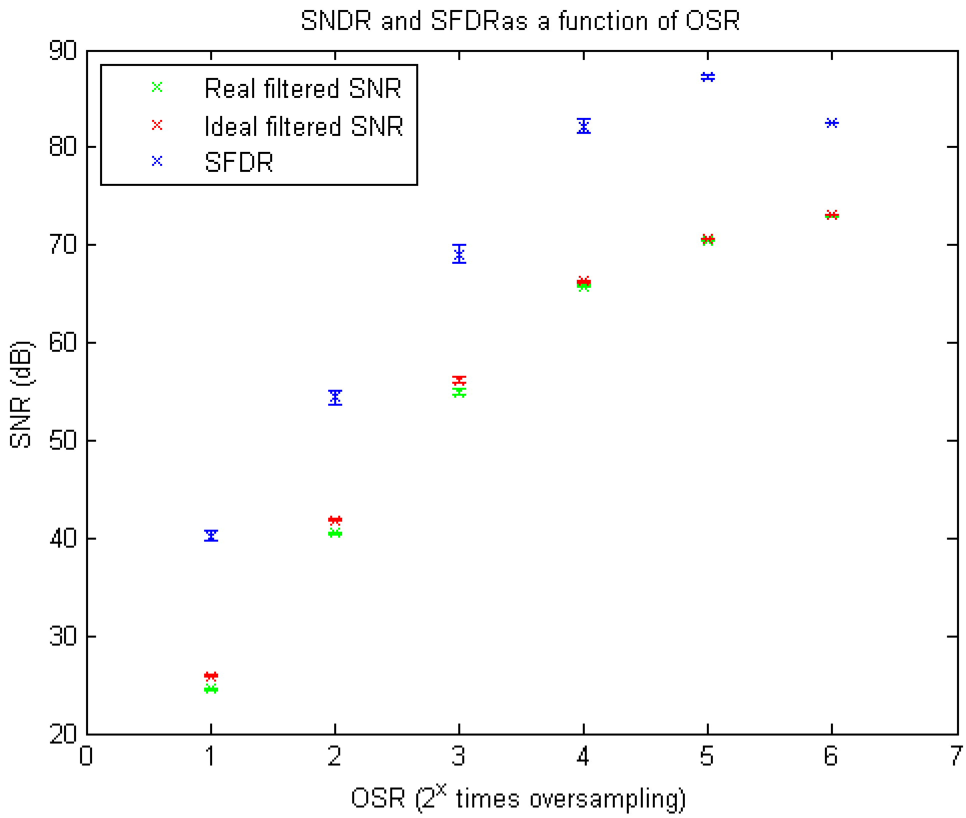

Figure 8: Results without Op-amp Offset Value, Input Amplitude=0.45, 10 Number of Simulations

The results below are achieved with all the non-idealities except op-amp offset are on with 10 runs. The input amplitude is 0.9:

SNR

OSR	1	2	3	4	5	6
	-0.5182	7.9865	52.4858	66.7447	76.1245	78.8008
	-0.7513	13.3387	52.5710	66.6355	75.7817	78.7789
	-0.6915	9.2986	52.8119	65.9695	76.0400	78.7450
	-0.9766	8.5775	53.0351	66.9270	76.1272	78.8099
	-1.1089	9.1612	53.1485	66.1244	76.0474	78.7304
	-0.4246	9.4504	52.2472	66.5360	76.0372	78.7584
	-1.4916	8.3499	52.4765	66.6468	75.7944	78.7567
	-0.3416	13.3561	52.9750	66.4789	75.9872	78.7773

-0.6421	8.6433	52.9573	66.0740	75.8399	78.7757
-0.4234	8.8089	52.2722	66.2135	76.0389	78.7772

SNR with Ideal Filter

OSR	1	2	3	4	5	6
	0.0910	8.0821	53.9414	67.9501	76.3607	78.9085
	-0.1041	13.4319	53.9966	67.7420	76.0202	78.8835
	-0.1292	9.4244	54.0710	67.2158	76.3704	78.8430
	-0.3080	8.6745	54.4551	68.0978	76.4281	78.9204
	-0.6658	9.2792	54.5015	67.4070	76.3150	78.8319
	0.1520	9.5463	53.5776	67.4473	76.3232	78.8622
	-0.7275	8.4442	53.9144	67.9406	76.0590	78.8571
	0.4998	13.4772	54.2837	67.6472	76.2471	78.8783
	0.0651	8.7525	54.2172	67.1786	76.0910	78.8852
	0.1282	8.8916	53.6763	67.4269	76.2852	78.8752

SFDR

OSR	1	2	3	4	5	6
	11.8166	19.6356	66.6771	80.4580	93.3099	88.2615
	14.0764	23.5541	68.4352	78.9208	91.0732	88.2595
	11.6132	20.5824	66.2331	78.0250	94.0271	88.2651
	12.3450	17.6721	66.6034	81.2271	93.6379	88.2636
	8.1952	19.5820	67.1812	78.7312	93.2308	88.2596
	12.0903	20.5715	66.3774	79.8206	93.1445	88.2588
	10.2215	19.4615	67.3868	78.4790	93.1538	88.2629
	11.5702	22.7394	67.7689	78.7030	93.8503	88.2593
	11.4931	18.4651	67.3433	79.5271	92.9735	88.2622
	12.1414	20.3792	67.6171	78.0789	93.3985	88.2628

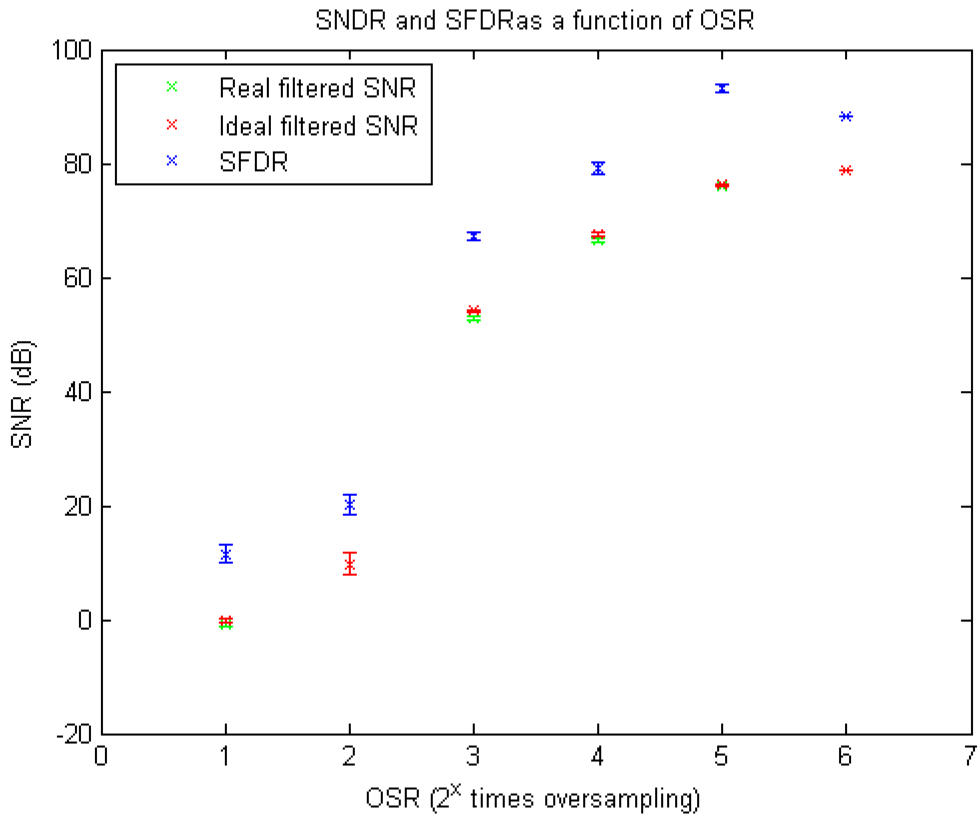

Figure 9: Results without Op-amp Offset Value, Input Amplitude=0.9, 10 Number of Simulations

The results below are achieved with all the non-idealities including op-amp offset are on with 10 runs. The input amplitude is 0.45:

SNR

OSR	**1**	**2**	**3**	**4**	**5**	**6**
	23.6692	37.4494	40.4984	40.6849	40.7027	40.7589
	24.1975	34.9338	36.2651	36.3550	36.3673	36.3388
	22.0097	27.8195	28.2114	28.2560	28.2646	28.2791
	23.0941	32.3822	33.1846	33.2379	33.2476	33.2282
	23.5303	39.1187	44.4700	44.8402	44.8731	44.7981
	23.8663	39.2445	45.2199	45.7220	45.7593	45.6760
	23.2458	32.3999	33.2309	33.2862	33.2961	33.2765
	23.7675	40.3711	52.0507	54.5495	54.7889	54.5911
	23.9341	34.1639	35.3903	35.4767	35.4882	35.5194
	23.3463	33.2631	34.3230	34.3855	34.3959	34.3734

SNR with Ideal Filter

OSR	**1**	**2**	**3**	**4**	**5**	**6**
	25.1295	38.0011	40.5312	40.6863	40.7028	40.7590
	25.3784	35.2323	36.2815	36.3555	36.3673	36.3388
	22.6933	27.8759	28.2132	28.2561	28.2646	28.2791
	24.2900	32.5596	33.1900	33.2381	33.2477	33.2282
	24.8428	39.8339	44.5571	44.8440	44.8735	44.7983
	25.5125	40.0149	45.3478	45.7263	45.7598	45.6762
	24.3707	32.5827	33.2370	33.2865	33.2961	33.2765
	25.5123	41.4684	52.4623	54.5835	54.7934	54.5924

	25.5539	34.4295	35.4015	35.4772	35.4883	35.5194
	24.5563	33.4499	34.3313	34.3858	34.3959	34.3734

SFDR

OSR	**1**	**2**	**3**	**4**	**5**	**6**
	37.8189	40.5096	40.6566	40.6990	40.7072	40.7612
	35.6822	36.2111	36.3343	36.3605	36.3689	36.3396
	27.5462	28.0827	28.2208	28.2568	28.2648	28.2793
	32.4761	33.0768	33.2143	33.2403	33.2484	33.2286
	37.0123	44.7554	44.8604	44.8777	44.8852	44.8039
	38.7325	45.6060	45.7505	45.7658	45.7734	45.6831
	32.6548	33.1302	33.2605	33.2888	33.2969	33.2769
	38.6302	53.5893	54.9243	54.8997	54.9067	54.6467
	34.7062	35.2918	35.4388	35.4814	35.4895	35.5201
	33.6638	34.2358	34.3624	34.3888	34.3969	34.3739

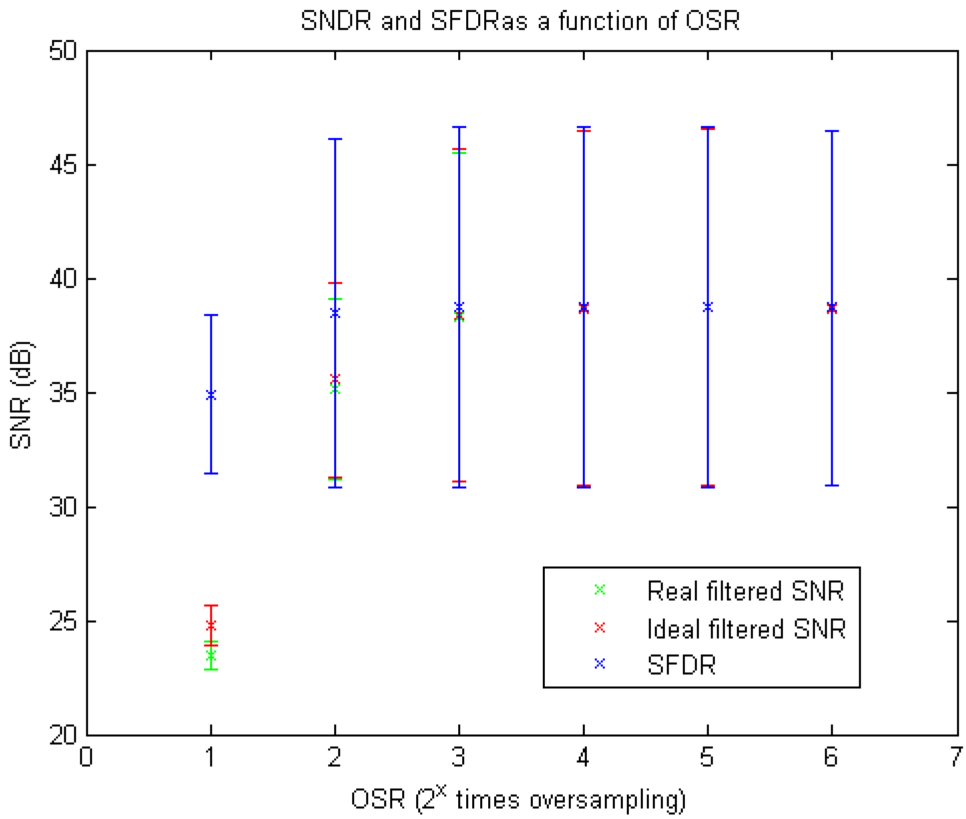

Figure 10: Results with Op-amp Offset Value, Input Amplitude=0.45, 10 Number of Simulations

The results below are achieved with all the non-idealities including op-amp offset are on with 10 runs. The input amplitude is 0.9:

SNR

OSR	**1**	**2**	**3**	**4**	**5**	**6**

5.6901	13.8758	35.8578	36.0072	35.9921	35.9734
3.3636	12.8104	41.6104	42.3980	42.4008	42.4309
5.7532	13.4100	36.6919	36.8837	36.8699	36.8839
4.6994	12.2353	39.9190	40.3047	40.2946	40.2663
6.2737	12.9985	40.2383	40.8416	40.8357	40.8058
5.2096	12.9447	48.0710	58.1239	58.9122	59.1773
4.2244	13.3340	48.2114	57.1011	57.7457	57.5898
4.4263	7.0926	39.6791	40.1473	40.1399	40.1621
5.7160	13.1046	34.2204	34.2752	34.2582	34.2422
4.7721	13.1564	44.3629	46.1559	46.1767	46.1256

SNR with Ideal Filter

OSR	1	2	3	4	5	6
	5.9288	13.9712	35.9305	36.0082	35.9922	35.9734
	4.1953	12.8757	41.8968	42.4032	42.4009	42.4309
	6.1761	13.4913	36.7676	36.8848	36.8699	36.8839
	5.2203	12.7004	40.0221	40.3072	40.2947	40.2664
	6.7899	13.0672	40.4394	40.8447	40.8358	40.8058
	5.7338	13.0272	49.3689	58.3004	58.9173	59.1784
	4.8580	13.4095	49.5687	57.2347	57.7491	57.5906
	4.9939	8.1036	39.8531	40.1500	40.1400	40.1621
	6.4483	13.1765	34.2586	34.2758	34.2582	34.2422
	5.2680	13.2229	44.7547	46.1664	46.1770	46.1257

SFDR

OSR	1	2	3	4	5	6
	17.3472	23.5719	36.0851	36.0119	35.9926	35.9736
	14.1741	23.6729	42.4863	42.4209	42.4027	42.4318
	19.0425	22.8486	36.9610	36.8892	36.8704	36.8841
	18.5331	22.3461	40.3963	40.3158	40.2958	40.2669
	20.1852	23.7067	40.9326	40.8565	40.8371	40.8064
	19.1832	21.1676	57.7224	59.0139	59.0008	59.2198
	16.6143	23.7209	57.9541	57.8362	57.8124	57.6193
	17.8149	16.2338	40.2267	40.1602	40.1410	40.1626
	17.0160	21.7164	34.3539	34.2777	34.2585	34.2423
	18.1660	20.4184	46.2821	46.2004	46.1811	46.1277

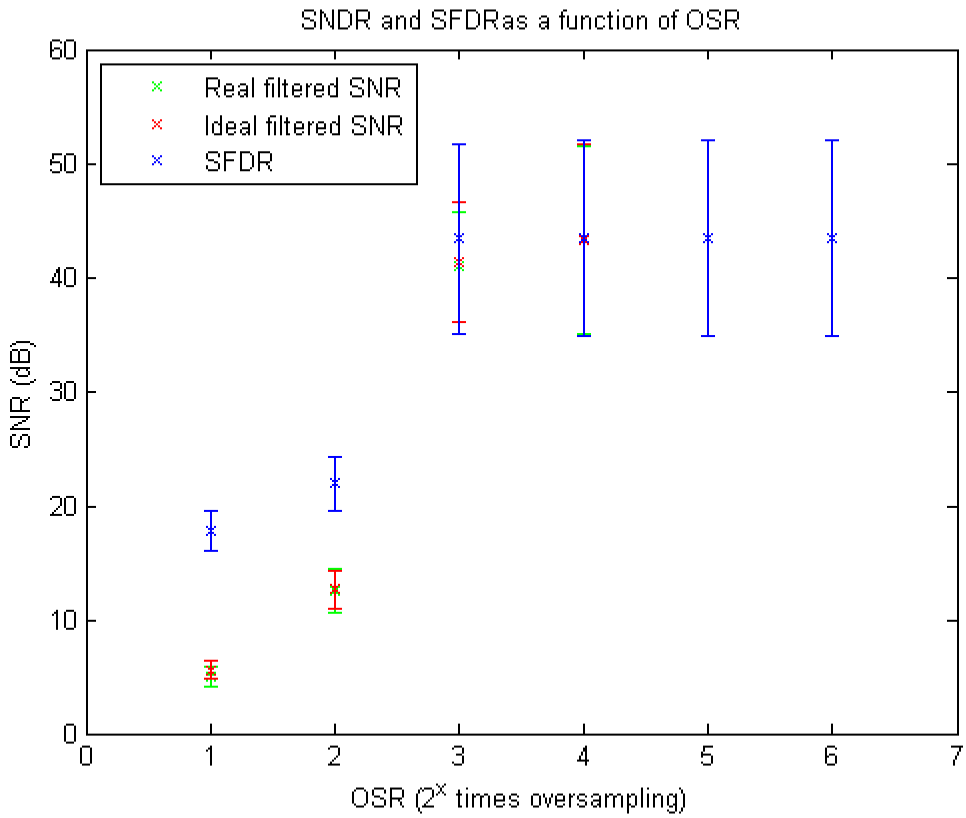

Figure 11: Results without Op-amp Offset Value, Input Amplitude=0.9, 10 Number of Simulations

The results below are achieved when there are no jittering, dithering, kt/C noise and interferer. Still the gain is non-ideal and comparator has an offset. The applied input has optimum amplitude of 0.7

SNR

OSR	**1**	**2**	**3**	**4**	**5**	**6**
	22.7574	41.5867	59.0573	72.7787	87.6639	100.2799

SNR with Ideal Filter

OSR	**1**	**2**	**3**	**4**	**5**	**6**
	25.6327	42.6703	59.7871	73.6872	88.5712	100.8173

SFDR

OSR	**1**	**2**	**3**	**4**	**5**	**6**
	32.3698	51.2547	69.8037	83.0390	96.7087	103.7543

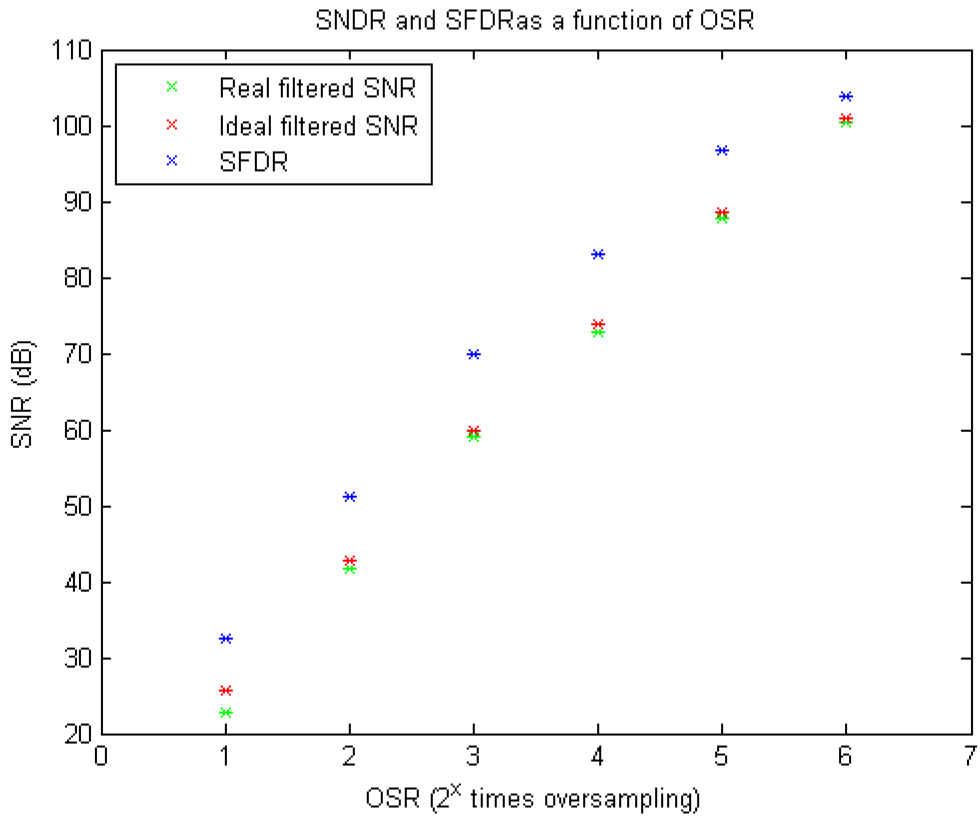

Figure 12: Results without Op-amp Offset Value, Jitter, Dither, kt/C and Interferer, Input Amplitude=0.7, Single Simulations

The results below are achieved from a single interleaving arm when there are no jittering, dithering, kt/C noise and interferer. Still the gain is non-ideal and comparator has an offset. The applied input has optimum amplitude of 0.7

SNR

OSR	**1**	**2**	**3**	**4**	**5**	**6**
	18.3615	34.4210	51.2719	65.7337	80.3742	94.9498

SNR with Ideal Filter

OSR	**1**	**2**	**3**	**4**	**5**	**6**
	21.4122	42.0472	55.7880	68.9470	84.9577	99.5908

SFDR

OSR	**1**	**2**	**3**	**4**	**5**	**6**
	23.8031	37.8020	61.0748	74.7257	90.9229	107.0300

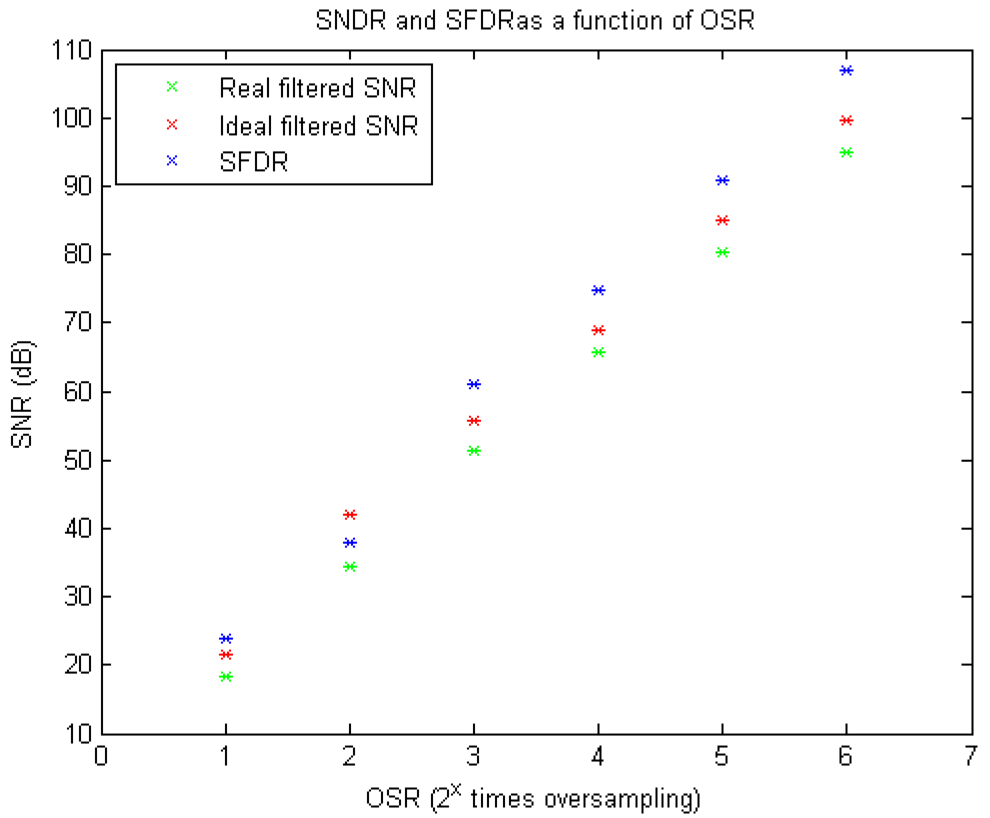

Figure 13: Results of Single Interleaving Arm without Op-amp Offset Value, Jitter, Dither, kt/C and Interferer, Input Amplitude=0.7, Single Simulations

5.b Frequency Spectrum

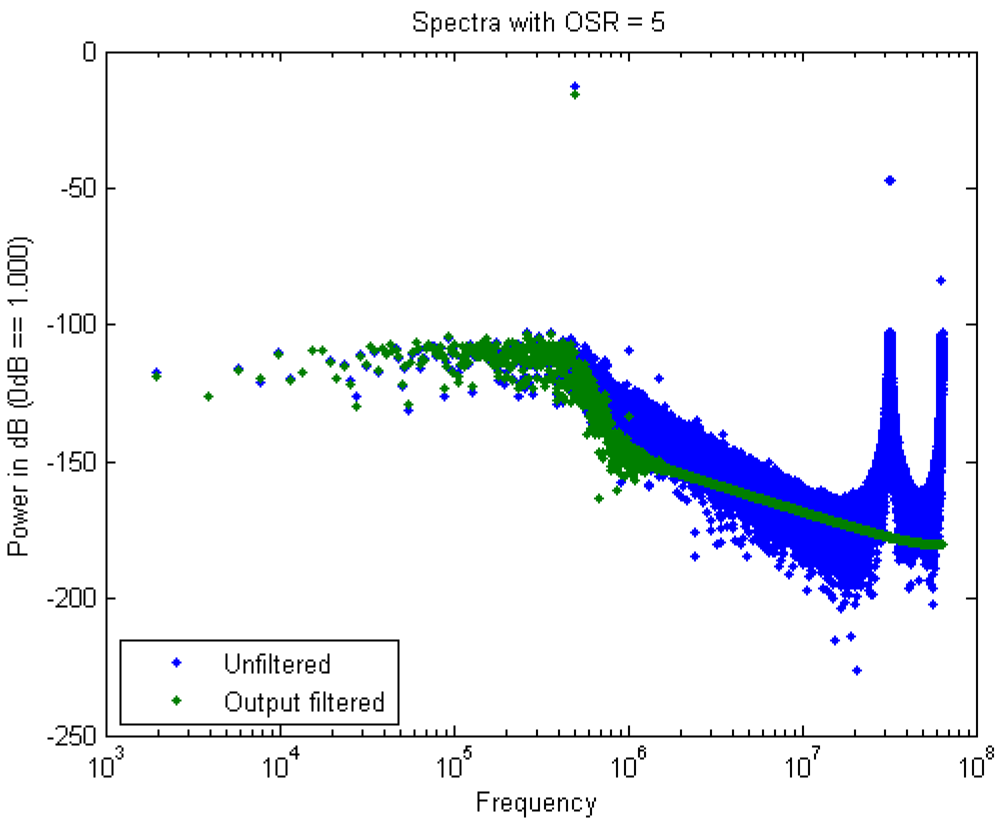

Figure 14: Spectra of the Output Signal (Input Amplitude = 0.45)

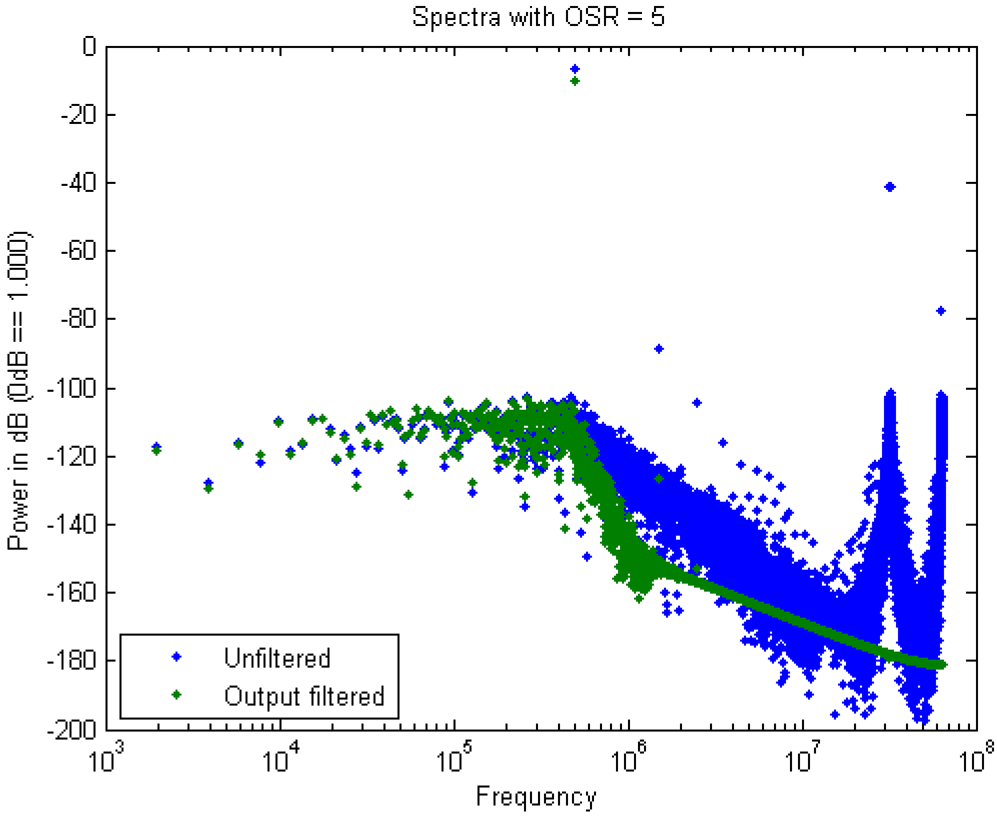

Figure 15: Spectra of the Output Signal (Input Amplitude = 0.9)

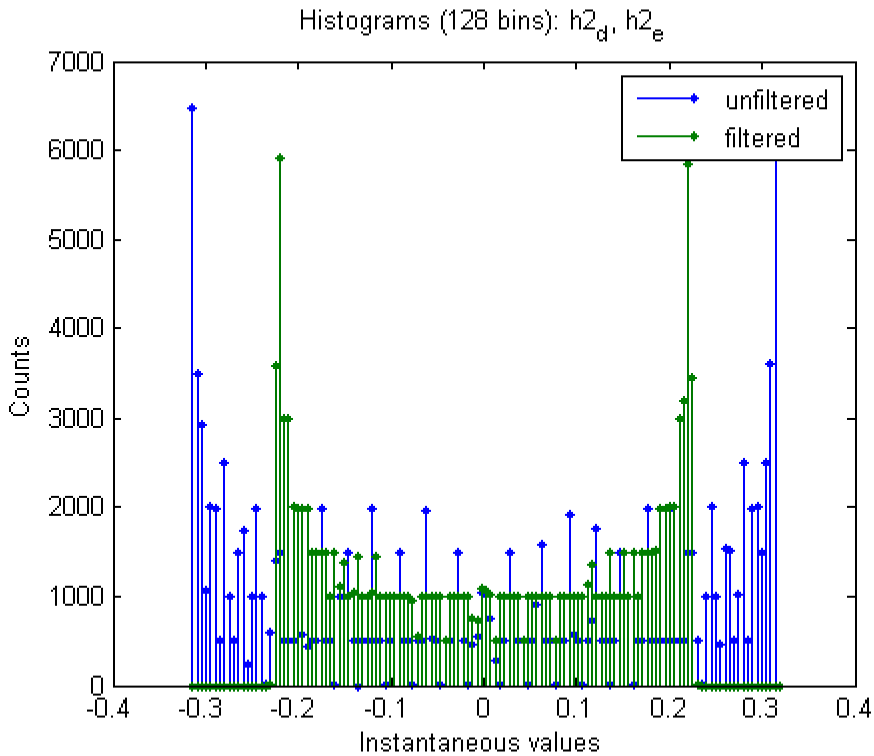

Figure 16: Histogram of the Output Signal (Input Amplitude = 0.45)

5.c Time Domain

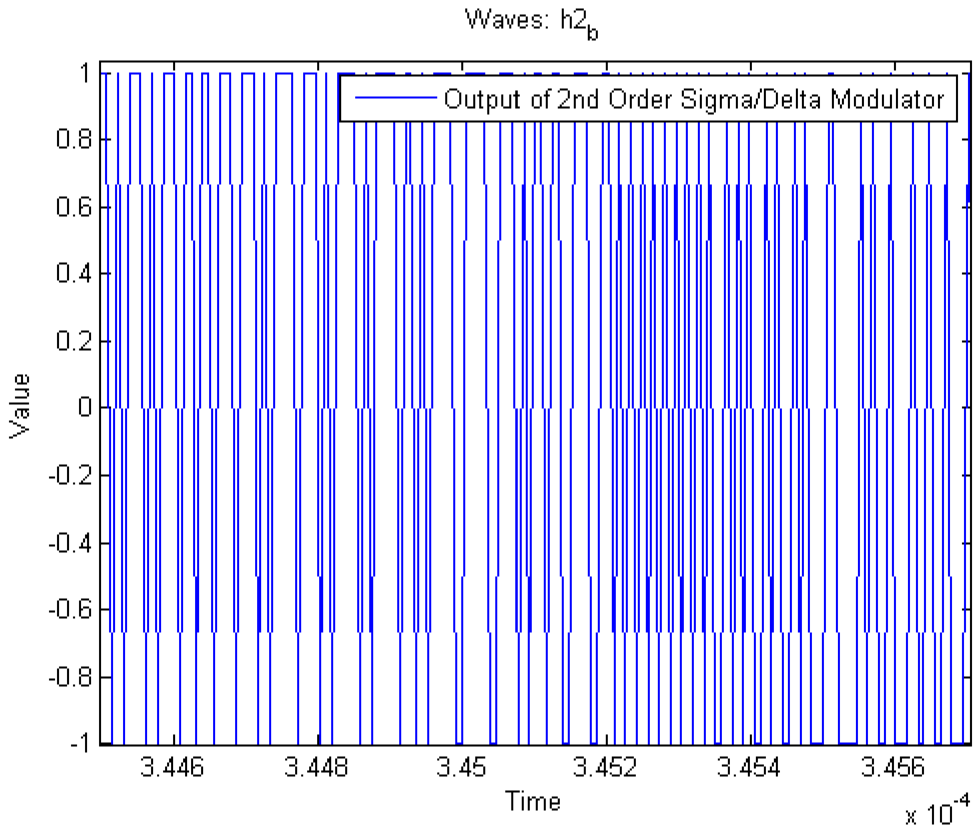

Figure 17: Signal after the Modulator

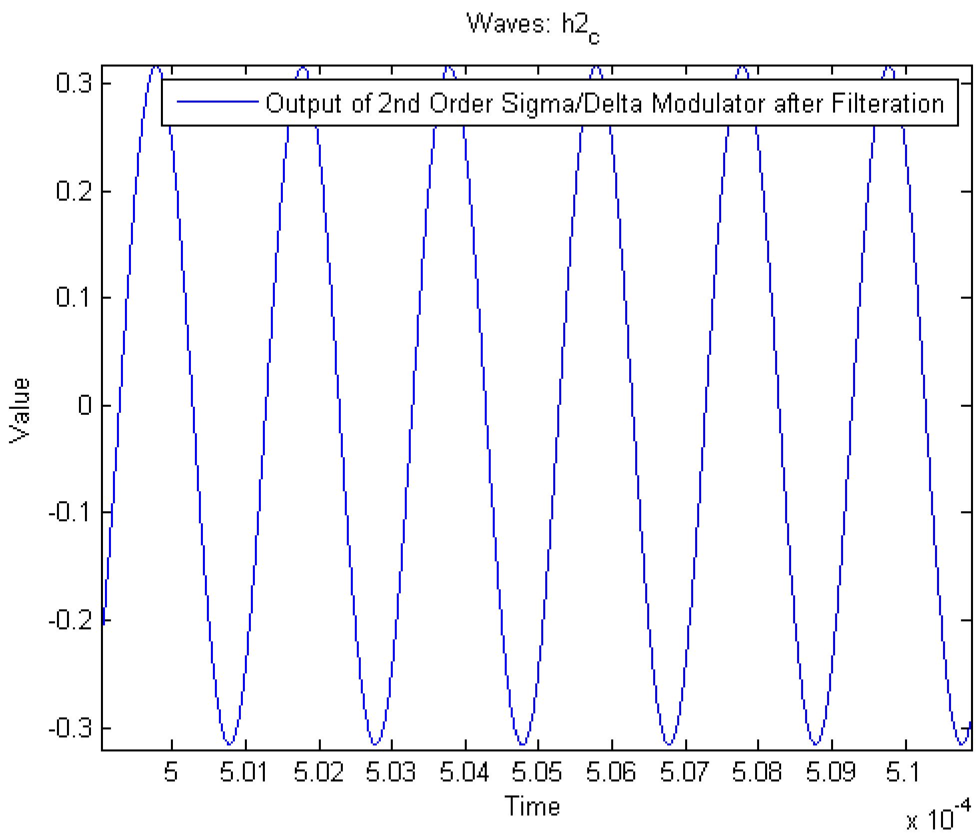

Figure 18: Signal after Noise Shaping Filter

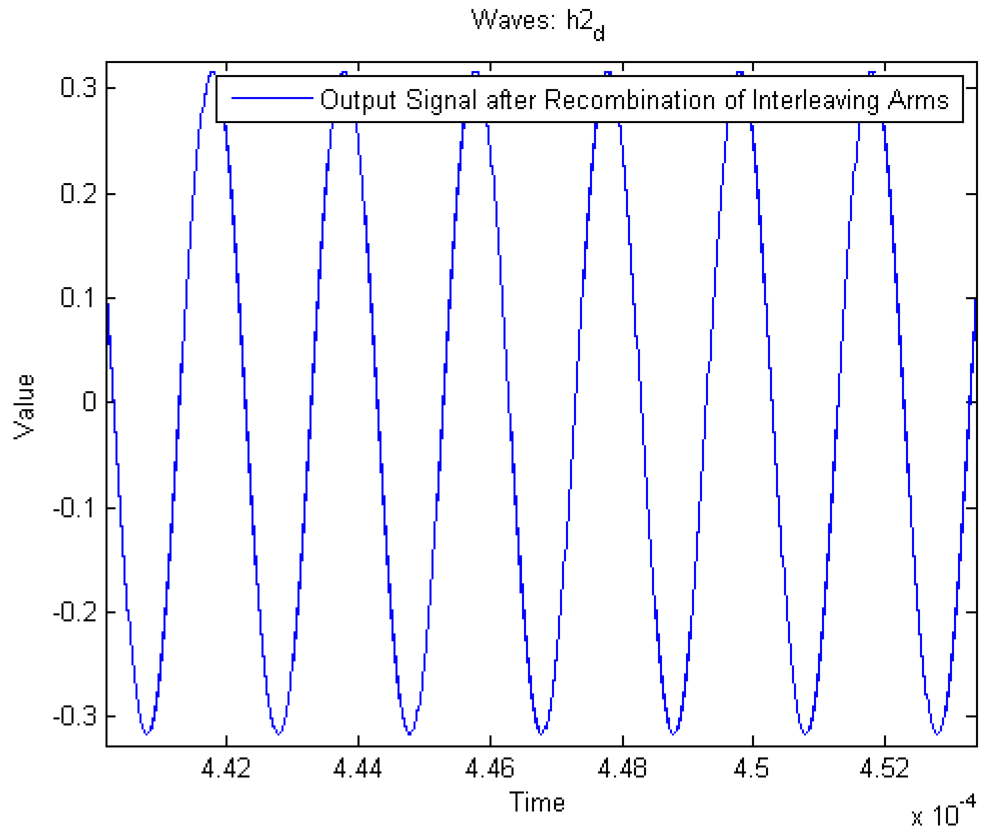

Figure 19: Signal after the Combination of Interleaving Arms

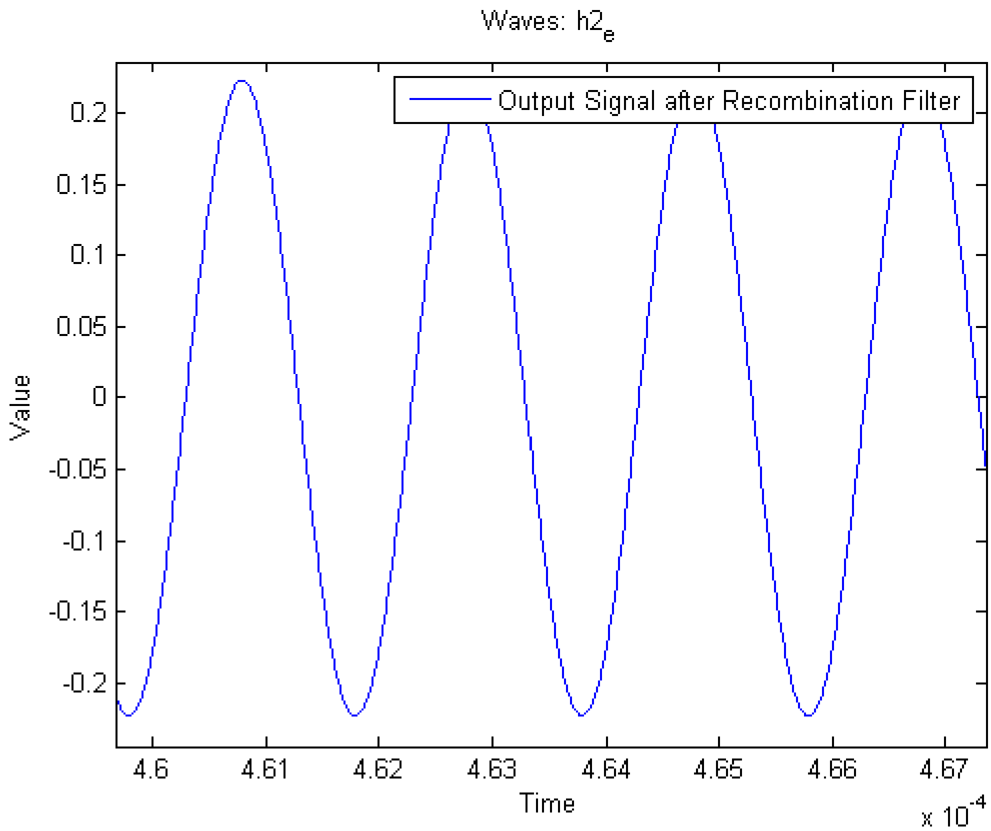

Figure 20: Final Output after Recombination Filter

6. Area and Power Estimations

A Matlab file is used for calculating the area and the power estimations. All capacitances are built with a unit capacitance of 0.5pF which gives a relative accuracy of 1%. Interleaving architecture takes more space but compensates the power dissipation by enabling the lowering of the clock frequency. Also it is assumed digital circuitry is free in both area-wise and power-wise.

Switching power: 0.0049766 W

Static power: 0.07 W

Total power: 0.074977 W

Total area: 55814 μm^2

7. Conclusion

Sigma/Delta modulators are powerful with their noise shaping feature yet due to oversampling the bandwidth of the input signal should be limited. On the other hand interleaving architecture can be used to provide some extra boost to the performance parameters, as it allows lower oversampling rates. Yet here the limitation is the area. Roughly it can be said that to increase the SNR by 3dB the area should be doubled.