ENS 492 Project Final Report

#007

MultiBand Operating RF Integrated Circuits / System

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Abstract

This project is made within the content of the courses ENS 491 and ENS 492, which are must courses for graduation in Sabanci University. In this project initially it is aimed to design a power amplifier operating in the regions of WLAN (2.4GHz – 5.4GHz) and WiMAX (3.6 GHz), using the Austria Microsystems SiGe 0.35µ BiCMOS HBT technology. The design process includes the finalizing the design for production.

The specifications for the design are:

- Linear Power Gain > 20dB
- Power Added Efficiency > 20%
- Output 1dB Compression >25dB
- S11 and S22 <-20dB

The project is completed in single band with some changes in specifications

Contents

1. INTRODUCTION

Freedom offered by the wireless devices is mainly limited by power amplifiers because of two main reasons. Battery life defines the amount of time in which the device can operate without being connected to an external energy source, and since power amplifiers are one of the parts of a wireless device that consume the most of the power, the efficiency of the power amplifier plays an important role on battery life. Moreover power amplifiers are one of the larger sized chips due to the use of passive components. Their size must be as small as possible in order to make the product small.

WLAN and WiMAX are two standards of wireless communication defined by IEEE. The lower frequency of WLAN defined by IEEE 802.11 b/g standards operates at 2.4 GHz on the other hand the upper frequency is defined by IEEE 802.11a standards operates at 5.4 GHz. In between these two frequencies exists WiMAX which is functioning at 3.6 GHz. Today cell phones and other wireless devices use these standards for different ways of communication. However to support these standards different circuits operating at different frequency ranges are required.

There are different concepts in designing a power amplifier covering the whole frequency range. First one is designing three different power amplifiers each working in another region and combining them parallel, this requires a lot of area and since products are made smaller this is not applicable.

Using varactors and other tuning elements proved to be unsuccessful due to the reasons that most tuning elements can not cover the wide frequency region and also the performance of the varactors are not linear within the required frequency limits. One can use resistors to design a matching circuit that can work on the whole frequency range however, since resistors mean loss, this method can not be used.

In this work initially it is aimed to achieve the multiband concept by using MOS switches changing between different LC matching circuits, unfortunately the idea could not be applied.

2. ABOUT POWER AMPLIFIERS

2.1 General Information On Power Amplifiers and RFIC Power Amplifiers

Power Amplifiers are the circuits whose aim is amplifying the power level of a signal in order to making the signal ready for transmission.

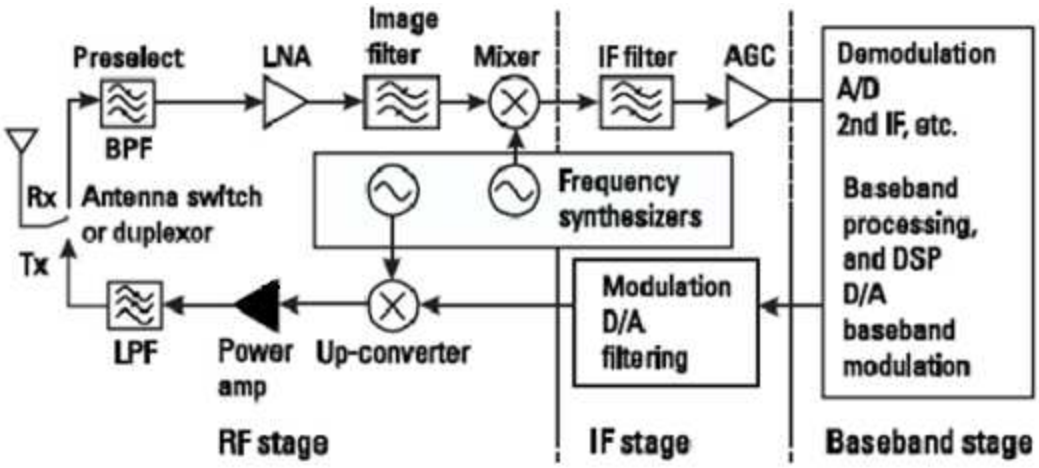

Figure 1: Generic Receiver Transceiver Block

In IC level there are other challenges with respect to discrete level. To start with, on chip inductors relatively take too much space and their quality factors are very low with respect to discrete elements. Besides due to the size of transmission lines large amount of losses are introduced in small lengths. In addition the breakdown voltage of the transistors limits the supply voltages, thus limiting the power that can be delivered to the output.

2.2 Power Amplifier Class Definitions

The transistor in an amplifier can be biased in different ways causing the transistor to operate in different modes. The classes define the maximum limits for efficiency. Here linearity is the payoff for the efficiency.

The classes of operation can be classified into three groups as linear amplifier classes, reduced conduction angle amplifier classes and switching mode amplifier classes. Linear amplifiers are class A, class B and class AB amplifiers. Reduced angle conduction amplifiers are class C amplifiers and switching mode amplifiers are class D, E and F amplifiers.

2.2.a Class A Amplifiers

In class A, the amplifier always conducts thus the output waveform is not distorted and is a sinus as the input. Class A has a conduction angle of 360° and has an ideal maximum efficiency of 50%

Figure 2a: Class A Operation, 360° of Conductance

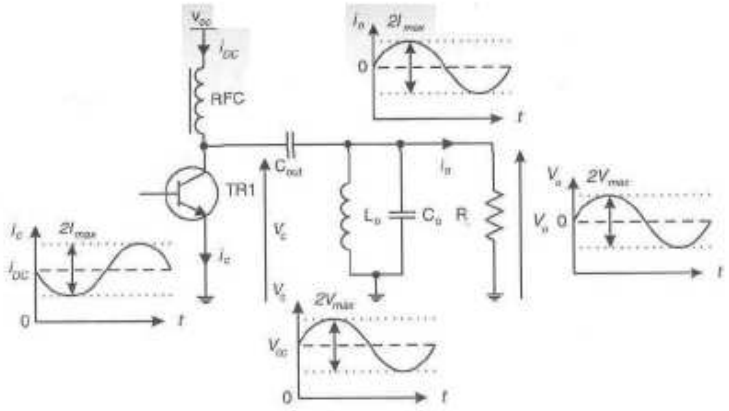

Figure 2b: Class A Operation Example

2.2.b Class B Amplifiers

Class B amplifier is designed such that it conducts the signal half of time only. This is done by biasing the transistor at cut-off. The input signal itself here activates the transistor. Class B transistor applies the idea of adjusting the DC power consumption with respect to the input signal, that's way class B amplifiers are more efficient than class A amplifiers. Here the conduction angle is 180°, and the maximum efficiency that can be reached is 78.5%.

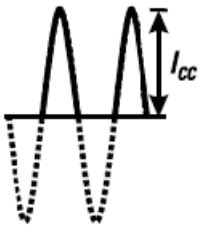

Figure 3a: Class B Operation, 180° of Conductance

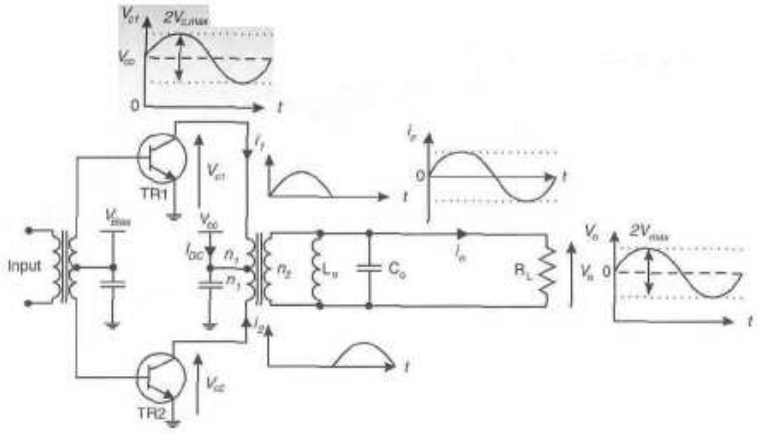

Figure 3b: Class B Operation Example

2.2.c Class AB Amplifiers

Class AB amplifier design aims to improve class A design's efficiency while not giving up the linearity as much as class B. The transistors are biased at a point between class A and class B. Thus the ideal efficiency ranges from 50% to 78.5%. And the conduction angle changes between 180° and 360°.

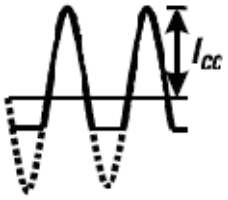

Figure 4: Class AB Operation, 180°-360° of Conductance

2.2.d Class C Amplifiers

The class C amplifiers employ the idea of reducing the conduction time of the transistor less then half of a cycle. With this the conduction angle is less than 180° and the efficiency ideally may reach 100% but at the limit 100% percent there would be no conduction. Here the output signal is totally distorted and it is a rather sharp signal with many harmonics, thus at the end of the amplifier there must be a filter in order to get rid of the harmonics.

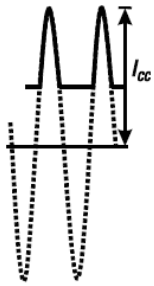

Figure 5a: Class C Operation, Angle of Conductance is less than 180°

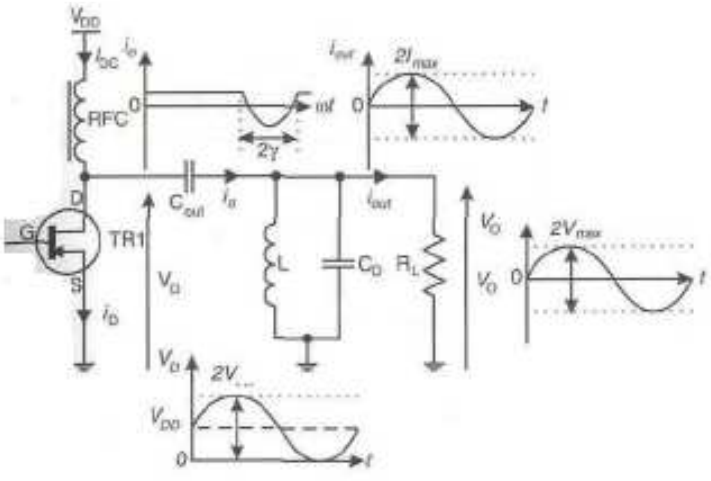

Figure 5b: Class C Operation Example

2.2.e Class D Amplifiers

Class D amplifiers use push-pull transistors via switching. Here the efficiency ideally may reach up to 100%. There are two versions of class D amplifiers voltage mode class-D (VMCD) and current mode class-D (CMCD). Here transistors are driven out of phase and both current and voltage exist at the same frequency in order to have only the fundamental frequency at the output. VMCD is used at frequencies at the MHz region and at higher frequencies CMCD is used.

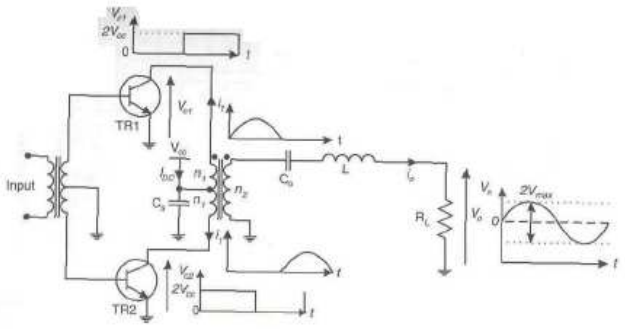

Figure 6: Class D Operation Example

2.2.f Class E Amplifiers

Class E amplifiers employ the idea of zero voltage switching (ZVS) which is aimed to lessen the loss due to switching. The transistors required for the class E amplifiers must have voltage breakdown larger than 3.6Vdd. Thus the transistors must be both fast and must have high breakdown voltage.

2.2.g Class F Amplifiers

Class F amplifiers are basically class B amplifiers that are overdriven by using harmonic resonators at the output in order to shape the signal. Their efficiency ideally may reach to 100%

2.2.h Conclusion On Classes of Amplifiers

The switching mode amplifiers are harder to implement as IC due to reasons such as the type of the required transistor or complex output circuits. Moreover these classes are aimed for efficiency purposes only and sacrifice a great amount of linearity.

In this project due to linearity concerns class A amplifier design is applied. However at the output stage where most of the power is to be delivered class AB is applied.

Moreover the classes of operation can be explained by Load-Line Theory. In the Ic vs Vce graph of a transistor, two points are chosen: In one the Ice is maximized which are at the knees of the curves. The other point is where the Vce is maximized and Ice is zero. Between those two points a line is drawn. The middle point shows the biasing point for the class A operation. Here since we have chosen the points so that one is (Imax,Vmin) and the other is (Imin,Vmax), when biased at the middle point we have a voltage swing of Vmax-Vmin and a current swing of Imax-Imin. By choosing different points for drawing load-line different classes can be achieved.

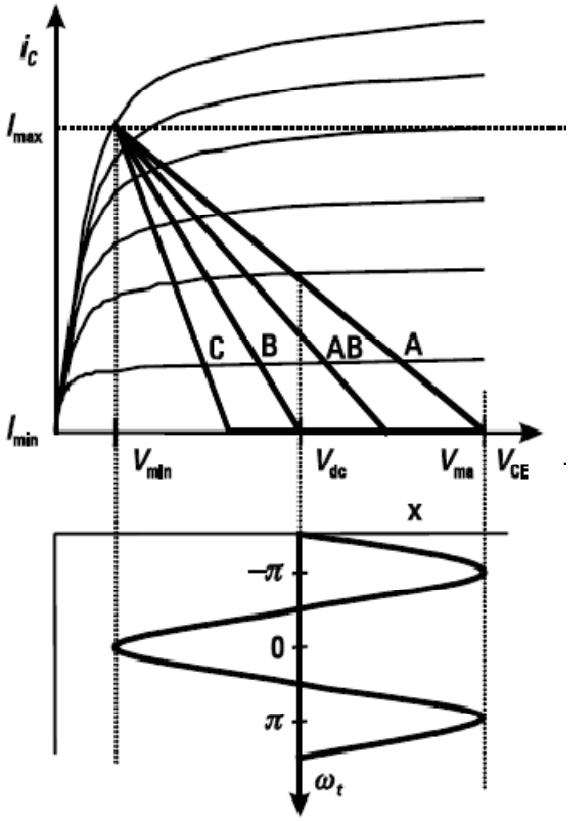

Figure 7: Classes of Operation with respect to Load-Line Theory

	Class A	Class B	Class AB	Class C	Class D	Class E	Class F
Ideal Efficiency	50%	78.5%	50%<, <78.5	<100%	100%	100%	100%
Conduction Angle	360	180	180<, <360	-	-	-	-

Table 1:Summary of Classes

2.3. Key Concepts and Challenges

Till here some concepts such as linearity and efficiency have been mentioned. However there are other challenges that must be overcome in order to make a successful design.

2.3.a Efficiency

As stated before the efficiency of a power amplifier is its one of the most important properties. Normally efficiency is defined as:

$$\eta = \frac{P_{\text{out}}}{P_{\text{dc}}}$$

However in amplifiers instead of efficiency power added efficiency is used. Power added efficiency (PAE) is defined as:

$$PAE = \frac{P_{rfout} - P_{rfin}}{P_{dc}} \quad \text{or} \quad PAE = \frac{P_{rfin}(Gain-1)}{P_{dc}}$$

2.3.b Linearity

Linearity is the relation between the input and the output. Ideally output is expected to change linearly with respect to the changes in the input, however due to biasing and operation mode of the transistor linearity may not be preserved causing thus causing distortion on the output. Ideally the output is defined as:

$$V_{out} = k_1 V_{in}$$

However in reality the output is a Volterra series:

$$V_{out} = k_0 + k_1 V_{in} + k_2 V_{in}^2 + k_3 V_{in}^3 + k_4 V_{in}^4 + \cdots$$

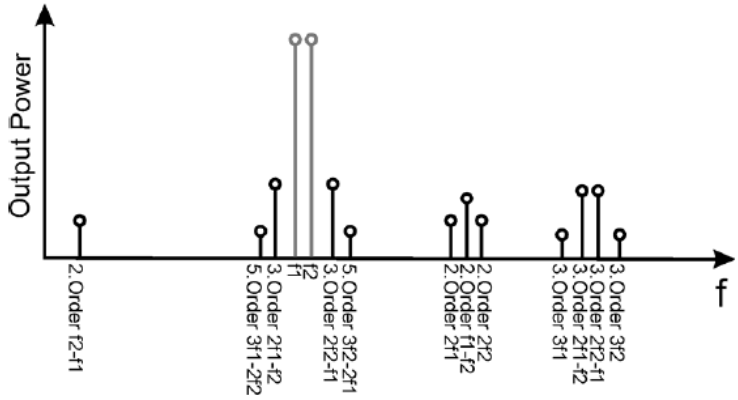

Figure 8: Output Spectrum Including Higher Order Effects

At some point the power of higher order products reach the desired output signal. For these issues compression points are defined to measure the device's linear operation range. 1dB compression point is defined at the point where the power gain is 1 dB less than the linear power gain. 1dB compression point can be defined both from input and output. If it is defined by the input, if the input power is equal to 1 dB compression level, then the gain is 1 dB less than the linear gain. On the other hand if it is defined from output, when the output power reaches 1 dB compression point, the gain is 1dB less then the linear gain.

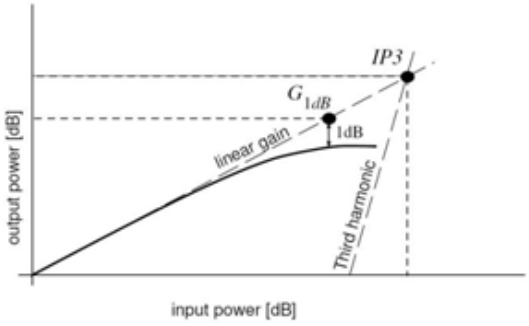

Figure 9: Linear Gain, 1 and 3 Compression Points.

2.3.c Power Gain

Power gain is the power difference in dB, between the input signal and the power delivered to the load. The power gain is related to the S21, and it is expected to be flat during the frequency band.

2.3.d Output Power

The main aim of the power amplifiers is to supply the required power to the load. Each communication medium has its standards defined by IEEE as the maximum power that is not dangerous to humans. For measuring power dBm is used rather than Watts.

$$P_{dB} = 10\log\left(P_{watts}\right)$$

$$P_{dBm} = 10\log\frac{P_{watts}}{10^{-3}\text{Watts}}$$

2.3.e Frequency of Operation

Each communication standard has it is own frequency range. A device working for a standard must operate successfully between these frequencies. For supporting WiLAN and WİMAX the power amplifier must work at the frequencies 2.4GHz, 3.6 GHz and 5.4GHz.

3. TECHNOLOGIES

There are many transistor types that can be used to make power amplifiers. Each of them has some advantages as well as disadvantages. The main concerns in power amplifiers are speed, noise and price.

3.1 Different Technologies

3.1.a Silicon (Si) Bipolar Junction Transistors (BJT)

Silicon BJT's supply high breakdown voltage, low price, easy production however they are limited in terms of frequency they reach as much as up to 5 GHz.

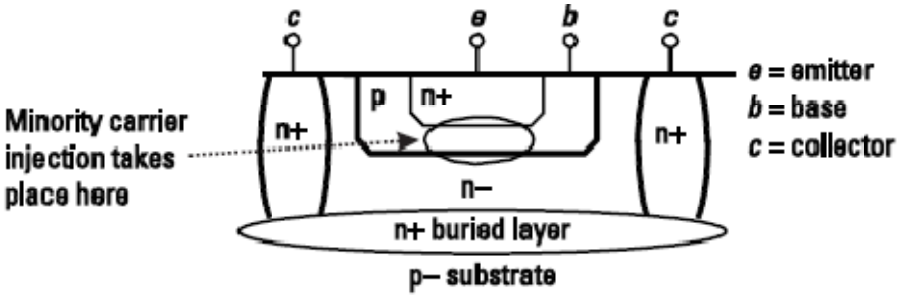

Figure 10: Cross section of BJT.

3.1.b Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

Even though MOSFETs are the dominant type in digital circuits, their speed and noise are not as good as BJTs. However the insulated gates provide better thermal structure and prevent the thermal runaway.

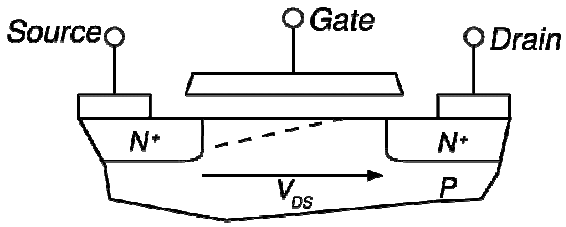

Figure 11: Cross section of MOSFET

3.1.c Literally Diffused MOS (LDMOS)

LDMOS are widely used in high power transmitters; they can deliver 120W at 2GHz. Since its source can directly be grounded, the feedback and parasitic due to bond wires are eliminated

3.1.d GaAs MESFET

GaAs MESFETs provide higher mobility thus can be used in higher frequencies. However its price is more than Si based transistors.

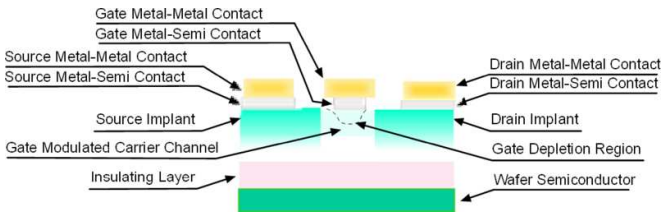

Figure 12: Cross section of MESFET

3.1.e SiC MESFET

The addition of carbon to silicon increases the mobility and breakdown voltage. SiC has speed comparable to GaAs and a far higher breakdown voltage than of GaAs MESFET around 10 times.

3.1.f HEMT

HEMTs are made by improving standard MESFETs. The schottky layer and channel layer are separated by AlGaAs and GaAs. This separation reduces the rate of collisions thus increases the mobility. The GaAS HEMT is also known as Modulation Doped FET (MODFET), (TEGFET), and Two-dimensional Electron-Gas FET (SDFET).

Also instead of GaAs other types of materials are used. In Pseudomorphic MESFET (pMESFET) instead of AlGaAs InGaAs is used, the addition of In further increases the mobility and the pMESFETs can be used up to 80GHz.

Moreover InP is used for further improvement. This results in lower thermal resistance and higher mobility. However their relatively low voltage breakdown prevents them from supply large amounts of power but they can be used up to 190GHz.

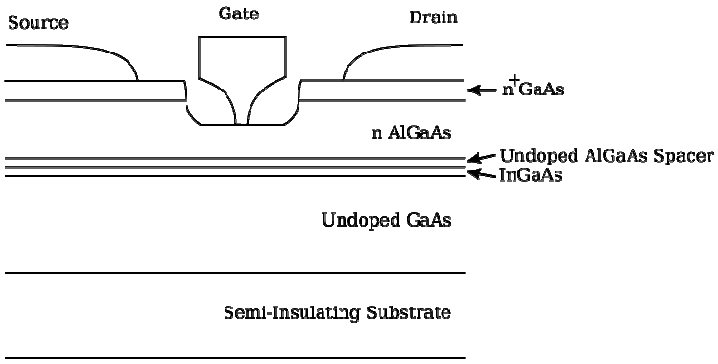

Figure 13: Cross section of HEMT

3.1.g HBT

HBTs have better mobility and parasitic. There are different materials used for producing HBTs. Rather than doping heterojunction is introduced as a barrier to allow better doping of the base to reduce base thus input resistance.

AlGaAs/GaAs, InP and SiGe HBTs exist. InP provides higher frequency response and better efficiency however due to pricing SiGe is also popular as it supplies great improvements over only Si devices, without giving up to much on production price.

3.2 AMS 0.35µ SiGe HBT

AMS 0.35µ SiGe HBT process has seven high voltage transistors defined as npn <c><b><e> h5. The transistors can be found in the library PRIMLIB and they are:

- npn111h5
- npn121h5
- npn132h5
- npn143h5
- npn232h5
- npn243h5
- npn254h5

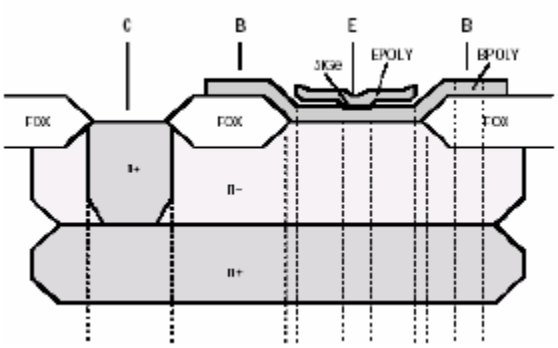

Figure 14: Cross Section of npn HBT of AMS SiGe 0.35µ Process

From these transistors npn254h5 is chosen as it allows the maximum area and due to its frequency response performance. The process allows 96 for the maximum area of the transistors. The transistors typically have a fmax of 50GHz. The transistors have typical collector-emitter breakdown voltage of 5.1V.

In analog design the most important limitations about a library is their inductors, since inductors are the least successful passive device to be integrated, most software can not simulate them and they contain the largest area in layouts.

The AMS 0.35 SiGe BiCMOS technology has 14 pre-designed spiral inductors that support the thick metal process. The inductors can be found in the library SPIRALS_4M. The information about the inductors is in table 2:

Inductor	Inductance			Qmax	Q		Fres(GHz)	Thickness(µm)
	Ls	**@2.4GHz**	**@5GHz**		**@2.4GHz**	**@5GHz**		
SP011S200T	1.07	1.04	1.05	11.9@4.4GHz	8.7	11.8	>6	20
SP015S250T	1.52	1.49	1.58	11.7@3.9GHz	9.6	10.2	>6	20
SP020S250T	2.02	2.04	2.17	10.4@3.9GHz	7.9	9.8	>6	10
SP021S200T	2.10	2.10	2.20	9.9@3.9GHz	7.8	9.3	>6	10
SP024S250T	2.42	2.42	2.75	9.6@2.7Ghz	9.3	6.5	>6	20
SP031S250T	3.07	3.17	3.63	8.9@3.0Ghz	8.4	6.6	>6	10

SP033S150T	3.25	3.32	3.52	9.4@4.3 Ghz	6.9	9.0	>6	5
SP037S250T	3.67	3.82	4.58	9.4@2.7 Ghz	9.0	6.2	>6	10
SP047S250T	4.66	4.90	5.98	8.3@3.7 Ghz	7.2	6.4	>6	5
SP049S300T	4.85	5.30	8.13	8.8@2.4 Ghz	8.6	3.7	>6	10
SP060S300T	6.00	6.59	10.09	7.2@3.0 Ghz	6.8	4.3	>6	5
SP073S250T	7.25	8.11	12.20	7.7@2.5 Ghz	7.5	3.2	>6	5
SP100S250T	10.02	12.08	19.23	7.2@2.0 Ghz	6.8	1.1	6	5
SP133S300T	13.30	19.06	-	6.7@1.7 Ghz	5.5	-	4.3	5

Table 2: AMS SPIRALS_4M Library

From the table it can be seen that the minimum inductance existing in the library is 1.08nH. However for the degeneration inductances, values lesser than 1nH are required. Degeneration inductances are crucial that they limit the gain and improve the output compression point.

Moreover the thicknesses of the metal paths determine the maximum amount of current that can be safely passed through it. AMS 0.35µm Met4 layer allows 5mA per µm of width. Thus the maximum current that can be passed over each spiral inductor can be calculated, whose maximum is 100mA.

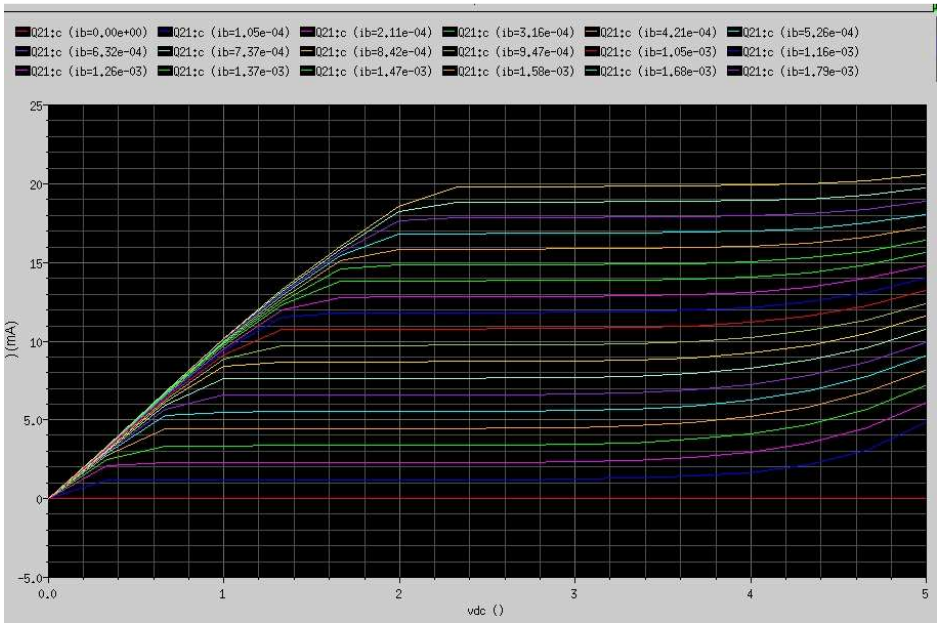

Figure 15: Family of Curves for npn254h5

4. Design Flow and Topology

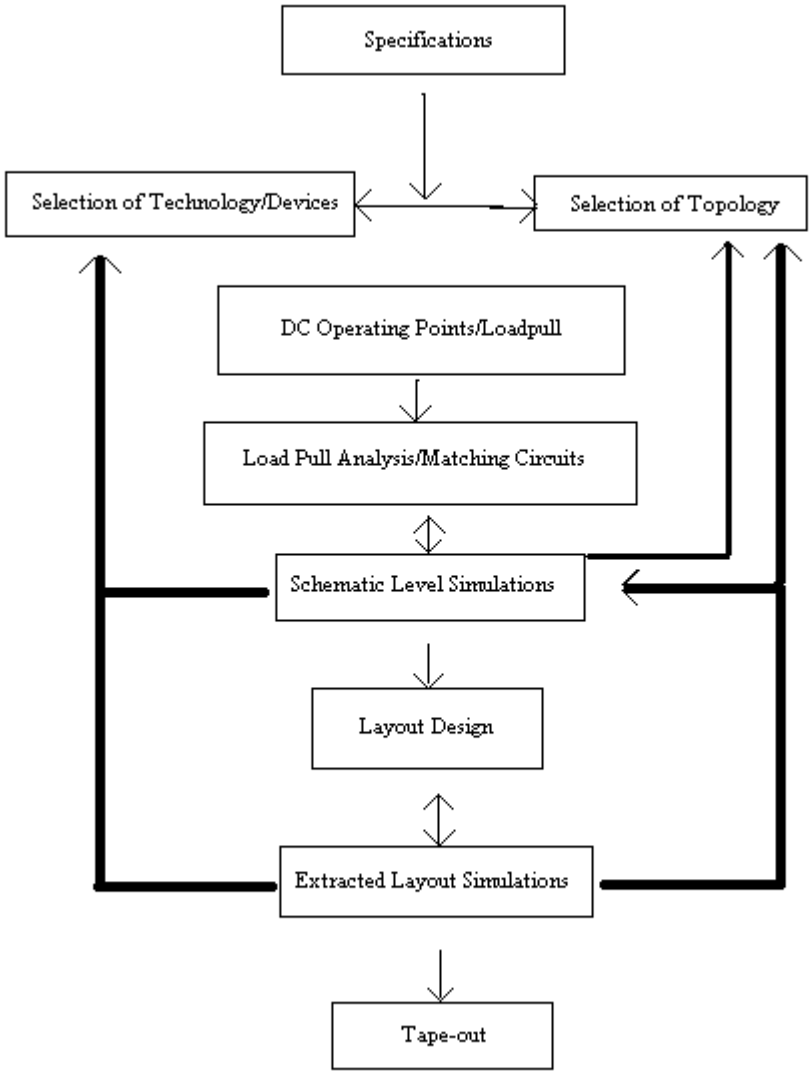

Figure 16: Design Flow Schematic

Design flow for the project. After simulations if the results are not satisfactory in the design flow back-steps are required. However the topology must be strong from the beginning.

For this power amplifier design a three staged topology is adopted.

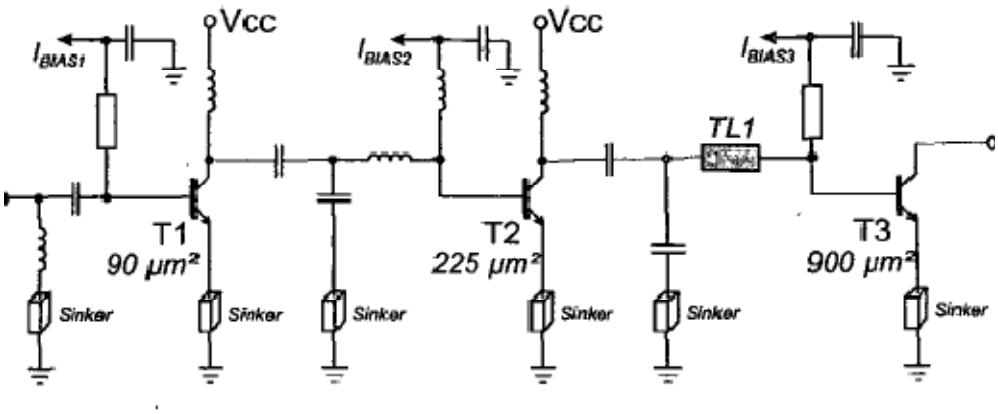

Figure 17: Schematic of an PA operating at 5.2GHz

Three stage design provides the necessary power gain which single stage designs can not provide. The first stage is the gain or driving stage, and the last stage is where the most power is created. The second stage while providing a respectful gain also helps the matching between two stages. Moreover this topology provides linearity since it does not include any switching activity.

5. SCHEMATIC LEVEL DESIGN

One of the most essential point is starting even schematic design with the knowledge of layout and production limitations. Such as the inductors of the process can carry at most 100mA with this one can not continue the schematic design by making current greater than 100mA pass through the inductors.

With layout concerns, while designing, the number of transistor which is defined by the area necessary for the specified output power must be of the order of two in order make the lines symmetric and in order to have a balanced current density, so that all the transistors will work properly after the fabrication.

With the equation:

$$Efficencypad = \frac{Output\ Power - Input\ Power}{DC\ Power}$$

Inserting power added efficiency as 25%, input power as 53.088mW (17.249dBm) and DC power as 3.3V*100mA (330mW) gives us output power of 136.16mW (21.39dBm) and gain of 4.15dBm at 1dB compression point.

To have a reliable circuit, the maximum current is limited to 80mA. Inserting the power added efficiency as 30%, input power again as 53.088mW (17.24dBm) and DC power as 3.3V*80mA (264mW) gives us output power of 130.96mW (21.17dBm) and gain of 3.93dBm at 1dB compression point. Thus the last stage's dc current is set as 80mA.

Moreover since in the schematic simulations all wires are ideal with no loss, capacitance and inductance, the power difference between the stages must be designed carefully so that after the RC extractions the connection between the stages of the amplifier should not be cut. To ensure that some power margin must be left between the input compression power of a stage and the output compression of the previous stage. However doing so decreases the efficiency of the design this should be done in order to make a working power amplifier. For this reason a margin of 2dBm is applied between the compression power levels of consecutive stages.

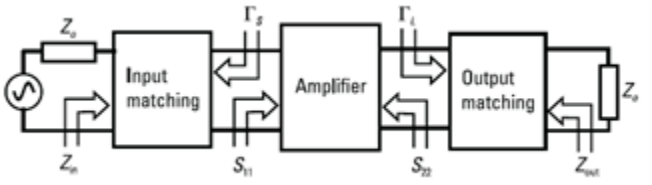

Figure 18: Reflection Coefficients.

For matching purposes L-type impedance matching is used. Because due to its simplicity the number of series element is one. Since the series elements can be either capacitor or an inductor and in reality they both introduce a finite resistance and loss, the power loss is minimized. Also for the same reason designs with series inductors are dismissed instantly.

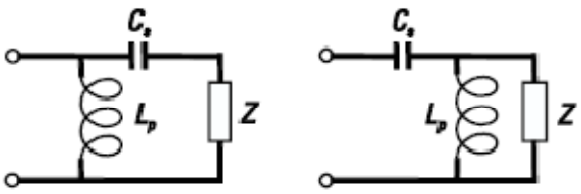

Figure 19: L Type Matching Circuits with Series C and Parallel L

The interstate matchings are done with a single series capacitor. Even though the input-output matchings are done at schematic level, they need to be done after the parasitics are extracted.

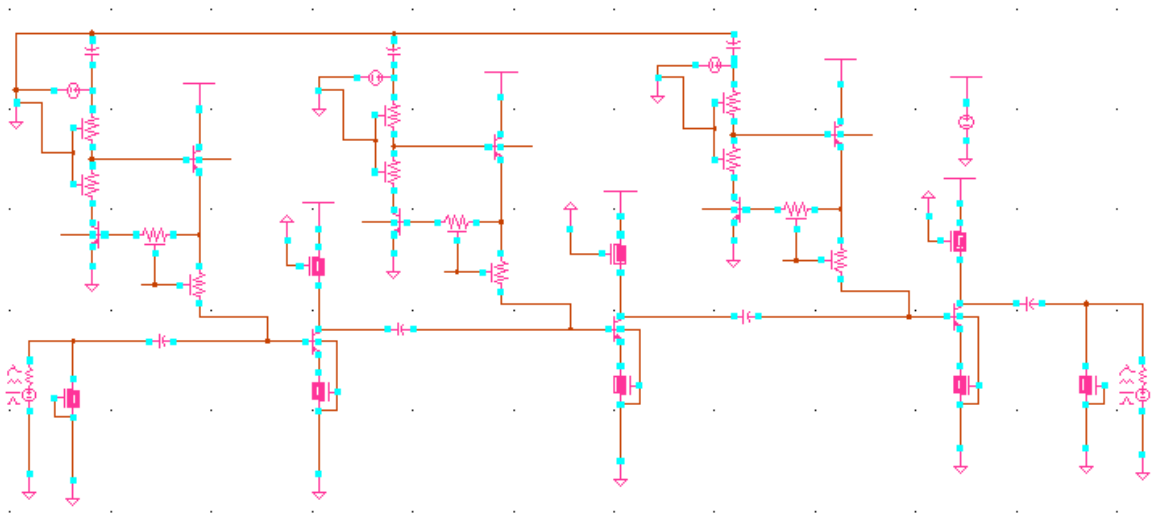

Figure 20: Schematic of the Power Amplifier

5.1 Schematic Level Simulation Results

Below are the simulation results at 3.6GHz are given

Input 1dB compression point: -1.85dBm

Output 1dB compression point: 20.78dBm

Power added efficiency at 1dB compression point: 18.11%

Linear power gain: 23.63dB

Even though each single stage has efficiency around 30%, after their connection this drops to 18.11% due to the 2dB power margin.

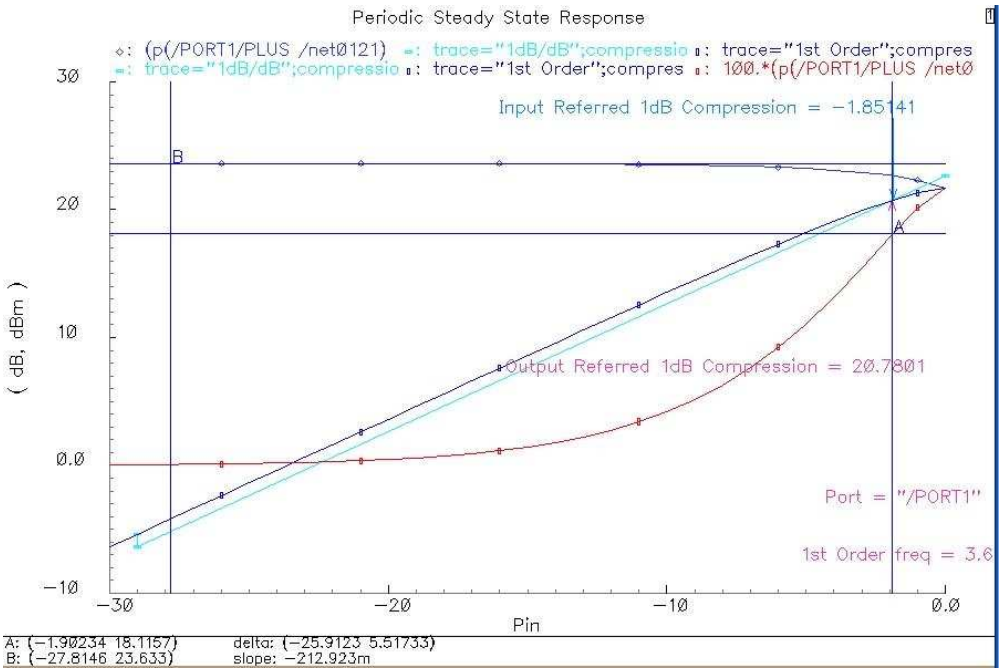

Figure 21: Power Related Schematic Results

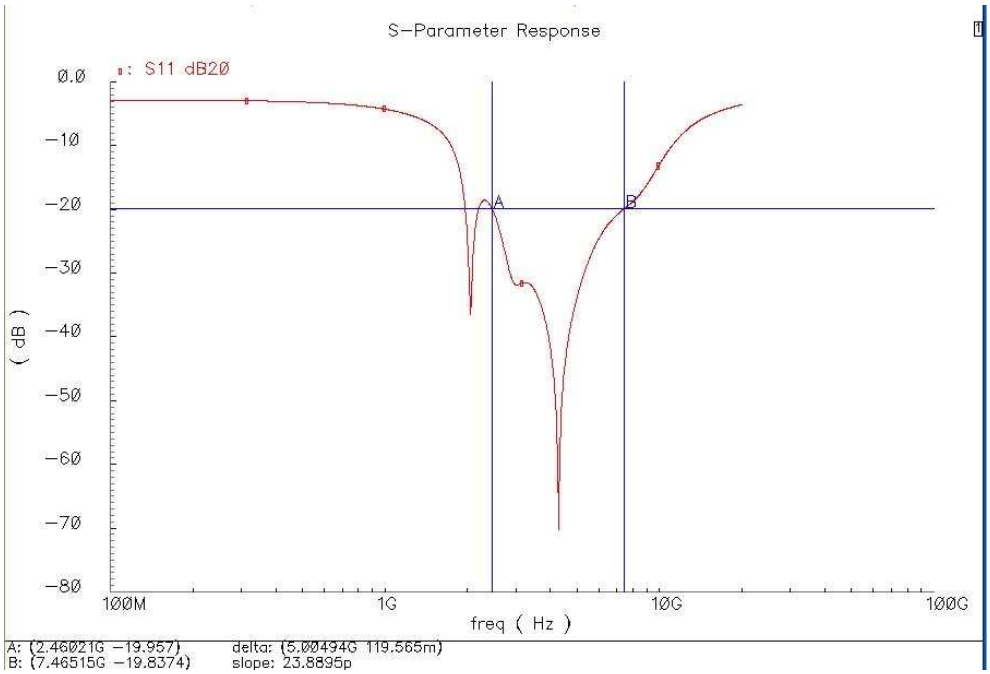

Figure 22: S11 Schematic Results

S11 parameter is defined by the input LC type matching. It is below -20dB between 2.46GHz and 7.46GHz.

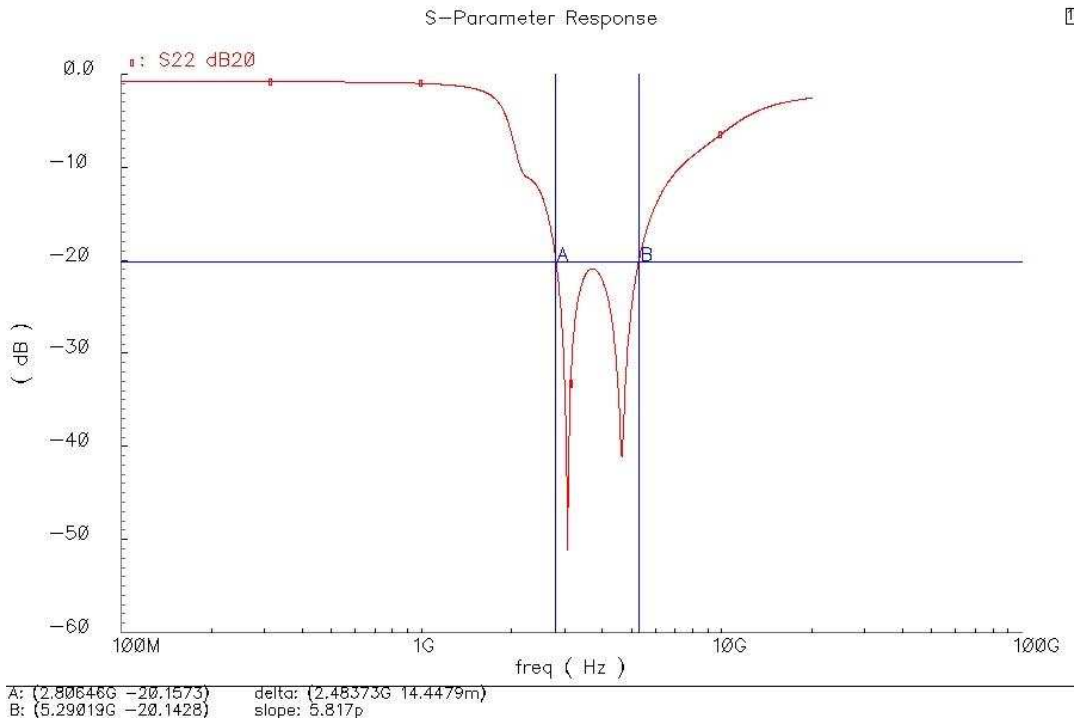

Figure 23: S22 Schematic Results

Output matching is done with a LC type network derived with help of load pull analysis. It is below -20dB between 2.8GHz and 5.29GHz.

The circuit inventory is defined as below:

First Stage:

2 transistors (npn254h5) with area 96u are used. Vdd is 2V since we are not trying to deliver large amount of power. In the emitters an inductance of 500pH is used.RFC inductor is SP020S250T. Collector DC current is 35.5mA.

Second Stage:

4 transistors (npn254h5) with area 96u are used. Vdd is 3.3V. In the emitters an inductance of 500pH is used.RFC inductor is SP020S250T. Collector DC current is 44.7mA.

Third Stage:

8 transistors (npn254h5) with area 96u are used. Vdd is 3.3V. In the emitters an inductance of 500pH is used.RFC inductor is SP020S250T. Collector DC current is 79.9mA.

Input Matching:

LC network with L=SP047S250T and C=3.69pF Cmim capacitor.

Output Matching:

LC network with L= SP024S250T and C=1.77pF Cmim capacitor. The output matching is done by using the load-pull analysis of Cadence Spectre tool. Load-pull analysis exhaustively scans all the possible load values and plots them in smith chart with constant power lines.

Simply matching the output to 50Ω may not give the optimum power or simply matching the output to another value which will give more power due to the formula below:

$$P = \frac{V^2}{R}$$

May result to very few amounts of power due to reflection which is defined as:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$

Since the created power can not be delivered to the load.

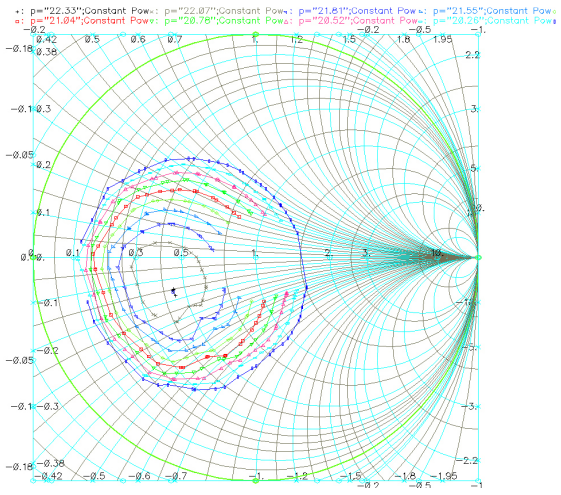

Figure 24: Result from Load-Pull Analysis

Biasing Circuits:

Each have 2 npn121h5 with 2u area, resistors of 600Ω,600Ω,15000Ω and a resistor with changing value in order to define the bias current. The biasing circuitry is fed with 2.8V in the first stage and 3.3V in the second and third stage.

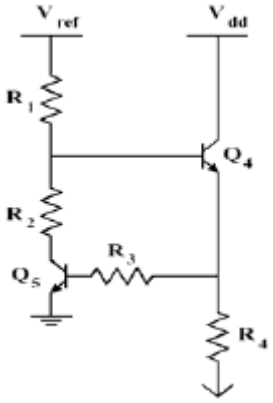

Figure 25: Schematic of the Biasing Circuit

The biasing circuit is a current mirror based circuit with two diode connected transistors. The current can be adjusted through the voltage divider and the reference voltage.

6. LAYOLUT LEVEL DESIGN

The layout is designed with the concerns stated in previous titles. Such that when the signal has to be divided, it is made sure that the paths are symmetric in order to have a homogenous current distribution and phase difference.

For this reason different routings has been tested for their performance. Here the problem was making a fully symmetric path tree was taking up too much space and since it is longer it was introducing more resistance and more loss.

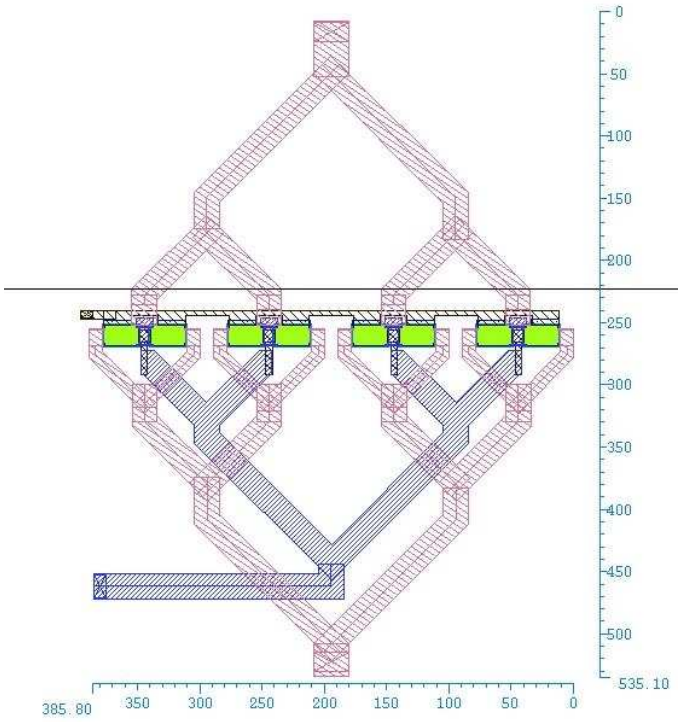

Figure 26.a: Transistor Paths, Full Symmetric

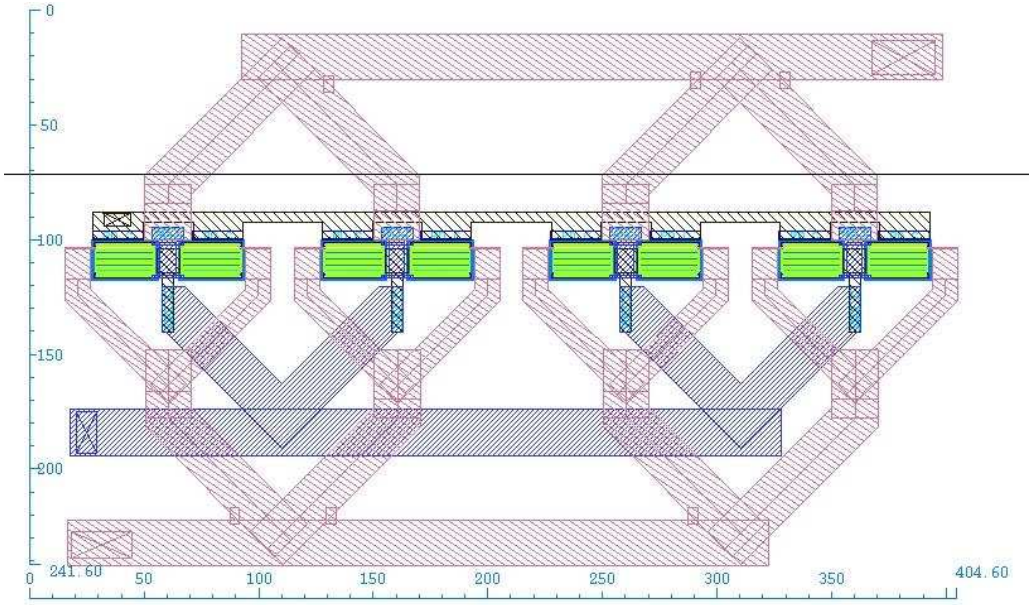

Figure 26.b: Transistors Paths, Hybrid

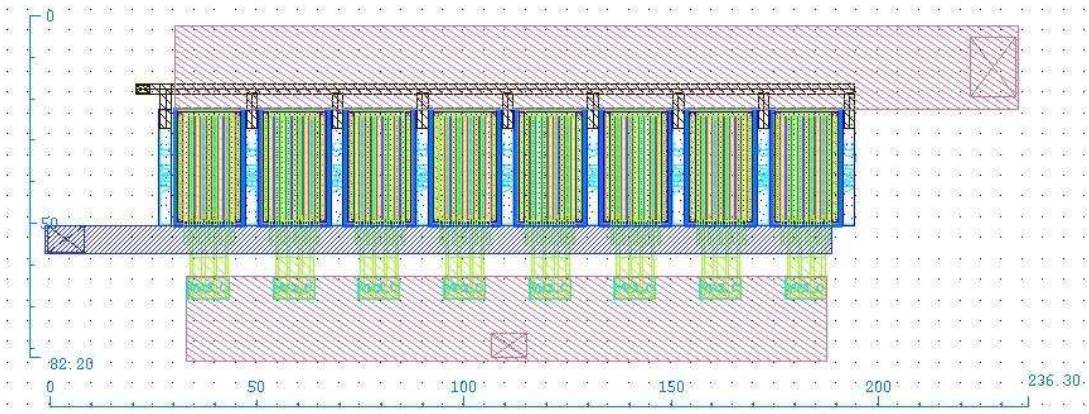

Figure 26.c: Transistor Paths, Small Area

From these paths path no b is used since it still has symmetry and introduced loss that is much less than the first one which caused 0.4dBm loss in the signal. Also it is area is much less than the first one. The third one is discarded due to the unreliability in the distribution of current. The current if not distributed equally may cause some transistors working compressed and some working less then they are designed.

However one of the most important concepts in RFIC design is grounding. For any device active or passive the grounding must be as good as possible in order to work correctly. Since working at high frequencies every small parasitic may effect the circuit. For this reason every empty space should be grounded and near every element ground must reach.

Also the capacitors have been placed between Vdd paths and ground in order to avoid damages due to RF leakage to these paths.

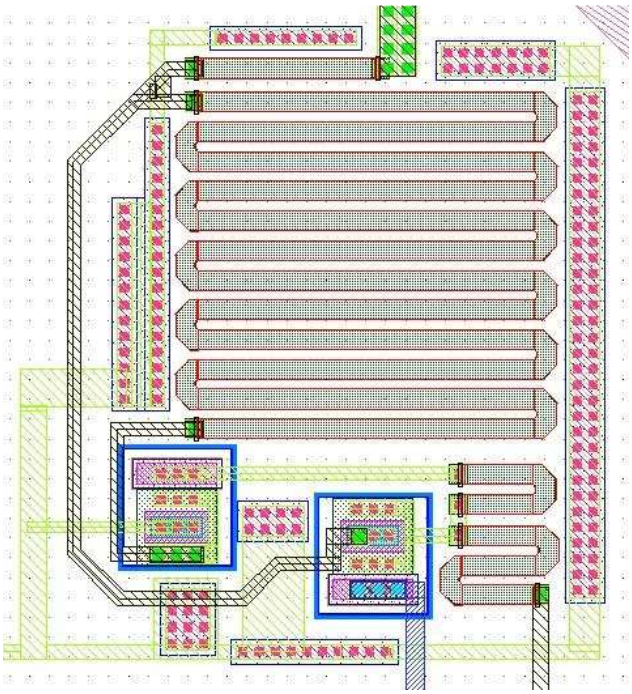

Figure 27: Layout of the Biasing Circuit

For the emitter degeneration inductors it is decided to design inductors using ADS Momentum. For the time being, the substrate file of the AMS SiGe 0.35µm process is being created by using the process documents of AMS. The layouts of the existing inductor designs from the library SPRILAS_4M has been drawn to the ADS Momentum, to check the correction of the simulation and the substrate file. After a successful process file which is confirmed by the data sheet of the inductors in the library is created from the datasheets of the AMS SiGe 0.35µm, inductors have been designed with consideration of the overall layout.

The equivalent circuit values are checked with the values taken from the RC extraction of the layout of the inductor, and for the simulation the extracted circuit is used with an ideal inductor whose value is given by momentum. This method is applied because even though most of the basic parameters like series inductance, quality factor, series resistance are similar with hand calculations and the simulator, there were some unexplained values.

ADS Momentum can make S-parameter simulations in which we can find the Z-matrix of a spiral inductor. The real part of Z11 corresponds to the resistive part of the inductor and the imaginary part of Z11corresponds to inductance and from their ratio one can find the quality factor.

Equations for results of Momentum;

Zr=real(stoz(S(1,1),50))

Zi=imag(stoz(S(1,1),50))

Q=Zi/Zr

Moreover by using the S-parameters that will be extracted from Momentum, it is aimed to find the values in the equivalent circuit.

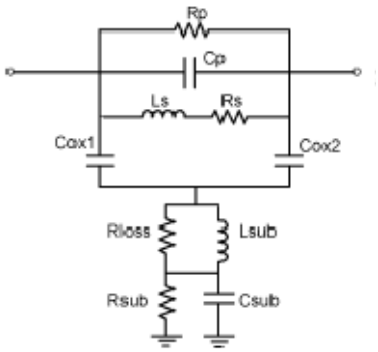

Figure 28: Equivalent Circuit

In figure 25, we see the equivalent circuit that is proposed to be more accurate than the more known ones. Here Rs and Ls are the serial resistance and inductance introduced by the spiral. Rp is introduced to represent the return path caused by the substrate. Cp is the capacitance occurring between the lines of the spiral that are parallel. Cox1 and Cox2 are the capacitance between the metal layer of the spiral and the substrate. Rsub and Csub are the resistance and capacitance seen due to the substrate. Rloss and Lsub are the elements that represent the power loss and loss due to heat while connecting to substrate.

The overall layout is about 2mm2 (2024µm*1070µm). The paths where most of the dc current will pass are fortified by using multiple layers of metal and used as wide as possible. The RF input and RF output pads have been modified from the standard AMS pads. Their unused metal layers are removed in order to decrease the parasitic capacitance introduced. This capacitance mostly affects the S11 and S22 parameters. The ground ring is drawn around the layout, and to avoid ground loop an empty space is left.

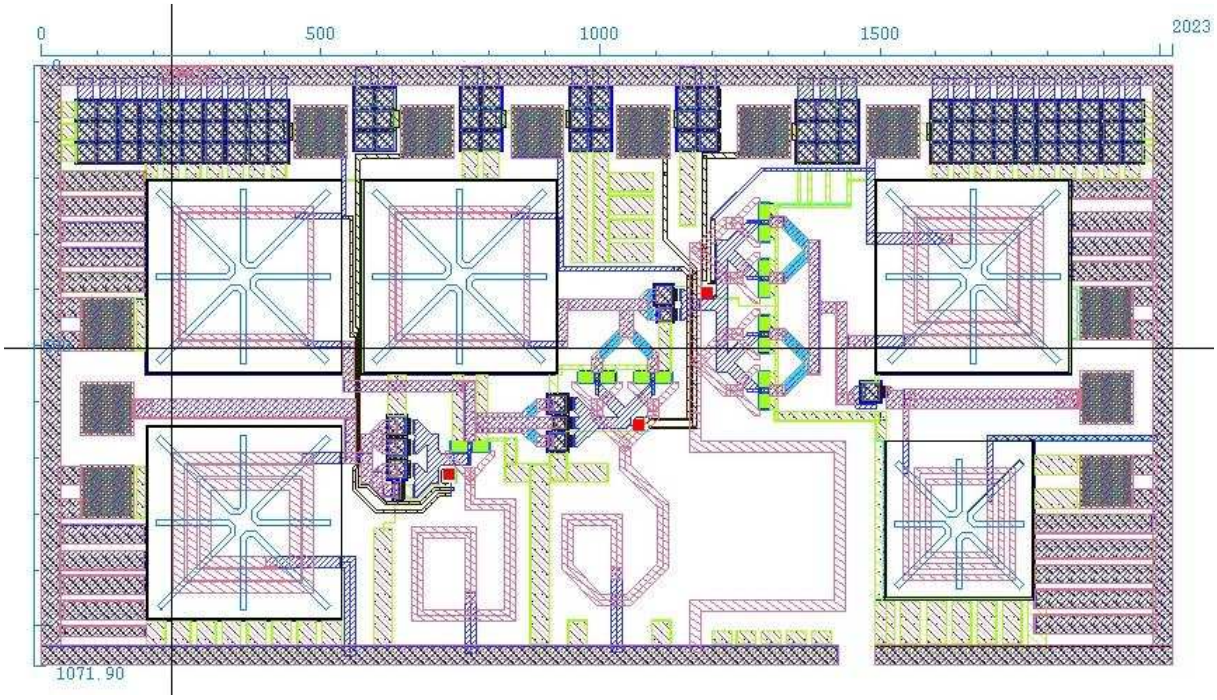

Figure 29: Final Layout DRC Rules Checked for Fabrication

6.1. Layout RC Extracted Simulation Results

Below are the simulation results at 3.6GHz are given

Input 1dB compression point: 0.71dBm

Output 1dB compression point: 20.72dBm

Power added efficiency at 1dB compression point: 17.56%

Linear power gain: 21.01dB

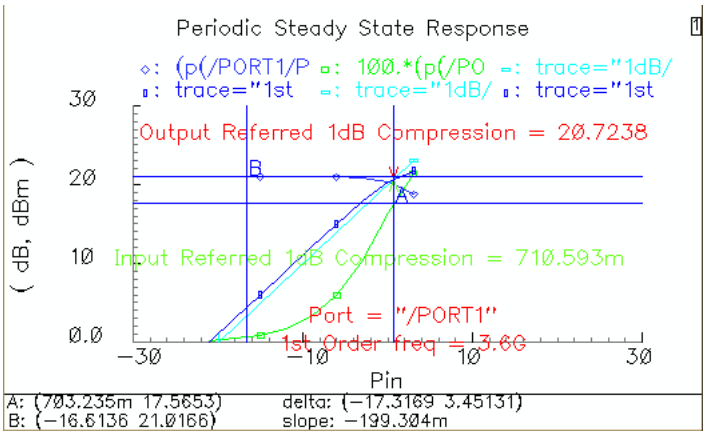

Figure 30: Power Related Results

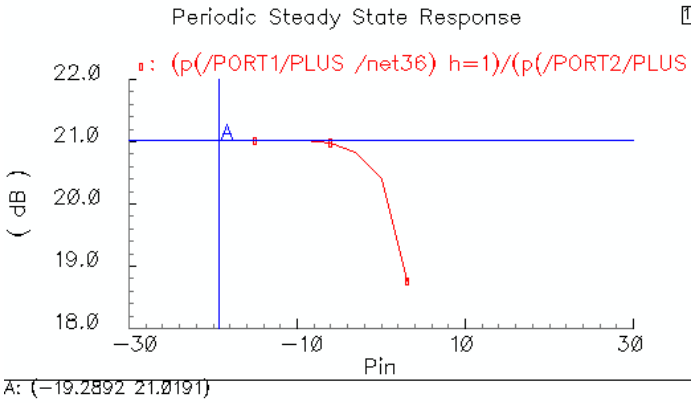

Figure 31: Power Gain

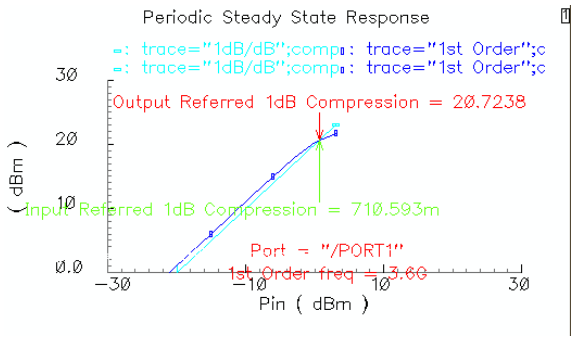

Figure 32: 1dB Compression Points

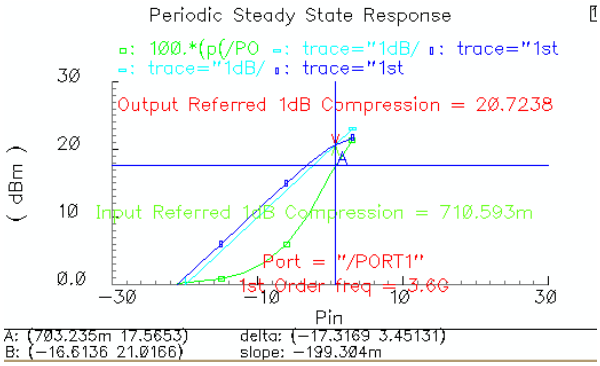

Figure 33: Power Added Efficiency

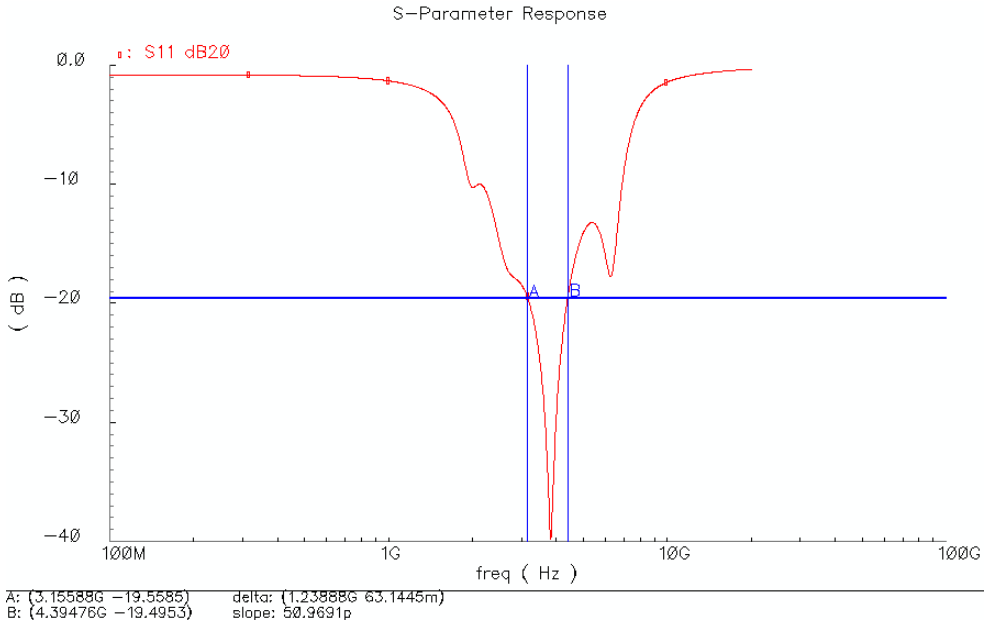

Figure 34: S11 Parameter

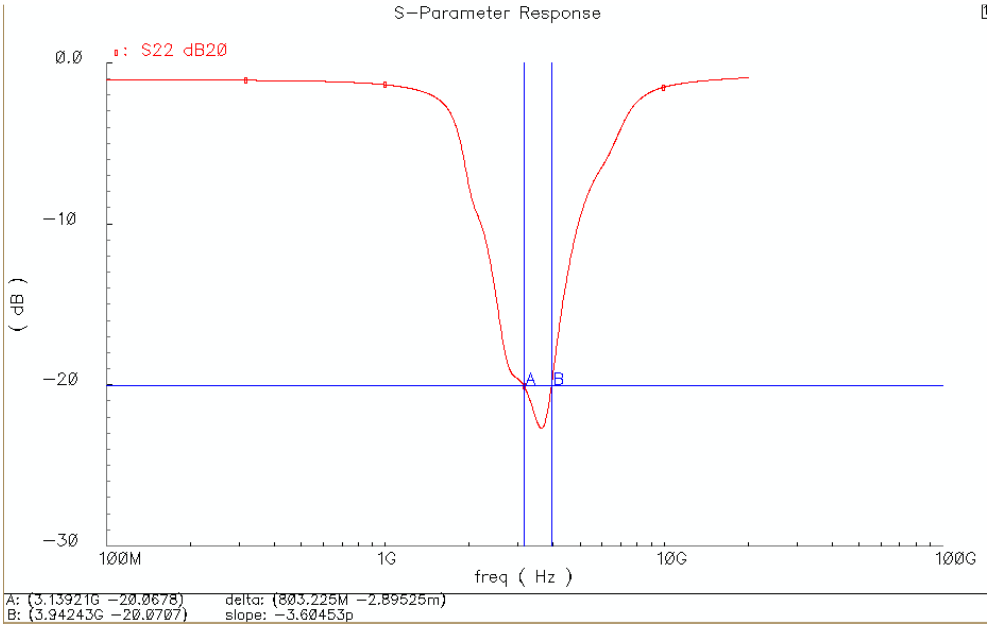

Figure 35: S11 Parameter

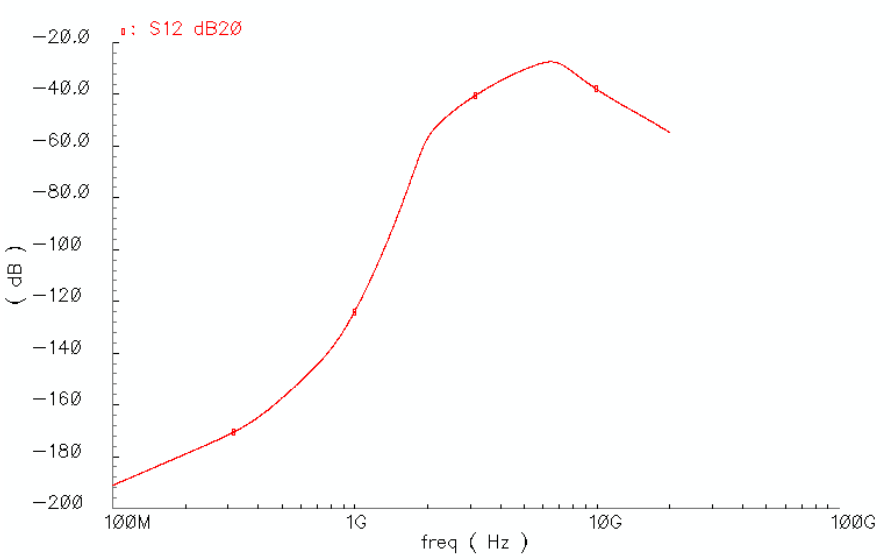

Figure 36: S12 Parameter

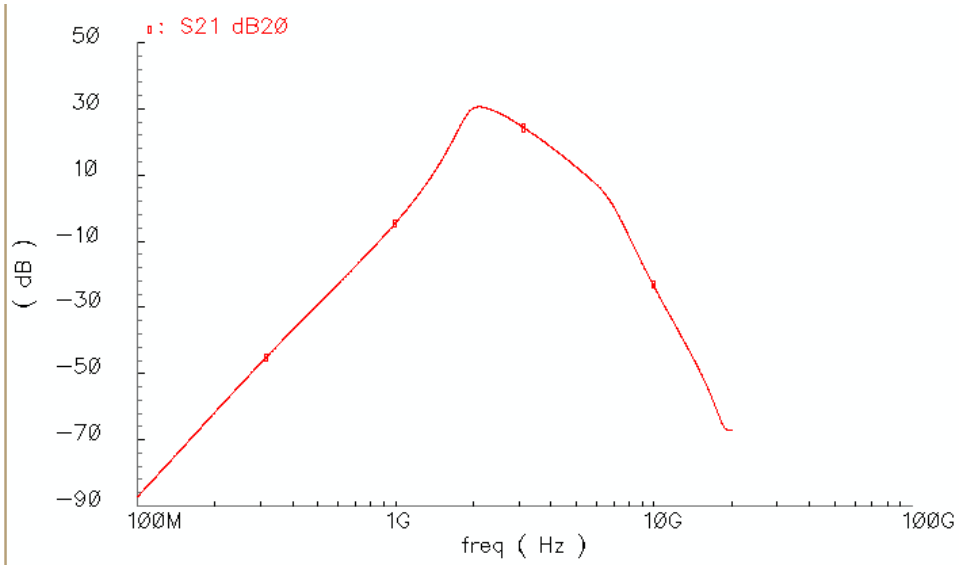

Figure 37: S21 Parameter

Here S11 below -20dB between 3.15GHz and 4.39GHz and S22 is below -20dB between 3.13GHz and 3.94GHz

7. FUTURE WORK AND CONCLUSIONS

7.1 Possible Future Work

For reliability the circuit is designed as passing current less than (80%) the maximum current the paths can carry. A design which uses the full current capacity of the paths may be designed. This will ideally increase the output power to 21.82dBm.

New inductors can be designed for RF choke that can withstand current enough to supply the desired output power of 25dBm.

7.2 Conclusions

During the flow of this project the challenges of a design that is made not for class purposes but that can match other products is seen. The process of designing a circuit for tape-out purposes is learnt.

With the project the combination of two previously learnt topics RF design and analog IC design is learnt.

	Input 1dB Compression	Output 1dB Compression	Power Added Eff. at 1dB Comp.	Linear Power Gain	Region: S11< -20dB	Region: S22< -20dB
RC extracted	0.71 dBm	20.72 dBm	17.56 %	21.01 dB	3.15GHz-4.39GHz	3.13GHz-3.94GHz

Table 3: Summary of Post-Layout Simulation Results

8. REFERENCES

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