EL 310: Hardware Description Design

Design Lab 4: Edge Detection Hardware

(Implementing Sobel Edge Detection Algorithm

using Verilog HDL)

R. Yağız Mungan (8288) & E. Selin Baytok (8088)

15. 06. 2007

INTRODUCTION

1) Implement Sobel edge detection algorithm on DIGILENT Spartan-3 starter development board.
2) The data-path may contain at most 4 adders other than the adders to take 2's complement.

Edge Detection and Sobel Algorithm

A rapid increase in the intensity of light at a certain pixel of the image is called as an edge. Its significance in image process comes from the fact that it indicates boundaries of the objects. This rapidity can be detected once the maximum and minimum points on the first derivative of the image. After the overall gradient vector is defined a threshold value is determined; if one of the pixel values exceeds this threshold, this pixel is noted to be an edge. Sobel algorithm is employed in order to determine an approximate value for the absolute value of the gradient.

In order to determine the absolute gradient value in 2D images Sobel algorithm implies two different convolution masks such as:

-1	0	+1
-2	0	+2
-1	0	+1

Gx

+1	+2	+1
0	0	0
-1	-2	-1

Gy

Fig 1. Sobel 2D Convolution Masks

Both Gx and Gy are slid over the image in x and y directions consecutively. On each 3 x 3 matrix these masks are applied mask values are multiplied with the corresponding image matrix element. The sum of these multiplications is placed in an output matrix.

The magnitude of the gradient is then calculated using the formula:

$$|G| = \sqrt{Gx^2 + Gy^2}$$

An approximate magnitude can be calculated using:

$$|G| = |Gx| + |Gy|$$

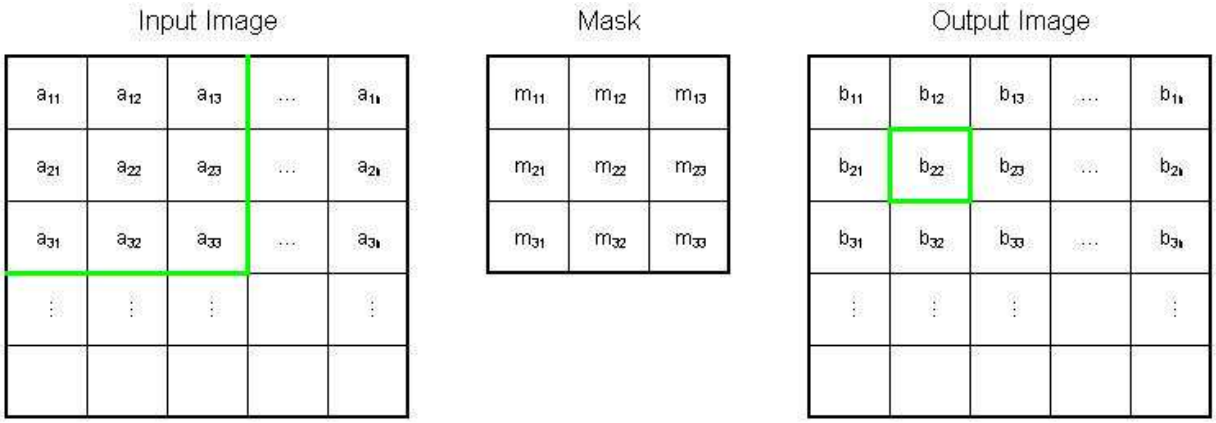

Fig 2. A Sample Detection Calculations

Pre-Design Decisions

Main challenge of the design was the limitation on the number of adders that can be used. In order to make the calculations with given adders it was required to build a state machine and design the sequence of parallel additions in groups of four.

Also the case of border pixel is concerned. Convolution masks could not be used for the first and last column and rows. They are considered to be unchanging.

In order to use the minimum amount of memory the number of matrix elements that are to be read from ram is tried to be minimized. For instance if a matrix in Fig 2 is read from ram for the first calculation then a12, a22, a32, a13, a23, a33 are kept in registers for the next calculation.

Flow of the Code

With the reset signal all the pointers that are used to extract the 3*3 matrices from the source are assigned their initial values:

```
y1<=0;
x1<=0;
y2<=1;
x2<=1;
y3<=2;
x3<=2;
```

Here x means x axis and y means y axis, thus x1,y1 refers to first column and first row. In 8 states of the FSM the matrix data are saved to registers and expended to 8bits. During the extraction of the last matrix element the additions start, since all the data required for the first 4 additions is already extracted.

```
M33<={8{data_out}};
Adder1in1<=X11;
Adder1in2<=X13;
Adder2in1<=X21;
Adder2in2<=X23;
 Adder3in1<=Y11;
Adder3in2<=Y12;
Adder4in1<=Y13;
Adder4in2<=Y31;
```

All the additions are completed in 4 states of the FSM. In the 4th state of the additions the approximation of the Sobel edge detection algorithm is applied. The absolute value is checked as follows:

```
if(out1[9]==1)
Adder1in1<=~out1+1;
else
Adder1in1<=out1;
```

In the last state (13th state) the output of the Sobel edge detection algorithm is saved to the 2nd ram by reducing the data to 1bit. Also the next state of the FSM is decided based on the current location of the extracted matrix with respect to the overall picture.

After all the data is written to the 2nd ram of the Spartan FPGA, the data is displayed to a monitor, through the ports of the FPGA which only allows black and white colours.

Multiplications and additions are made combinational, however assigning of the inputs are made sequentially.

Conclusion

In this project the skills of finite state machine design with limited sources and programming the design in Verilog programming language were improved, while an understanding of edge detection and especially Sobel Edge detection algorithm was developed.

Appendix A

Synthesis Report

Release 6.2.03i - xst G.31a

--> Parameter TMPDIR set to __projnav

CPU : 0.00 / 3.31 s | Elapsed : 0.00 / 1.00 s

--> Parameter xsthdpdir set to ./xst

CPU : 0.00 / 3.31 s | Elapsed : 0.00 / 1.00 s

--> Reading design: el310_top.prj

TABLE OF CONTENTS

==========

* Synthesis Options Summary *

==========

---- Source Parameters

Input File Name : el310_top.prj

Input Format : mixed

Ignore Synthesis Constraint File : NO

Verilog Include Directory :

---- Target Parameters

Output File Name : el310_top

Output Format : NGC

Target Device : xc3s200-4-ft256

---- Source Options

Top Module Name : el310_top

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

FSM Style : lut

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

ROM Style : Auto

Mux Extraction : YES

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : YES

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

Resource Sharing : YES

Multiplier Style : auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Equivalent register Removal : YES

Slice Packing : YES

Pack IO Registers into IOBs : auto

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Keep Hierarchy : NO

Global Optimization : AllClockNets

RTL Output : Yes

Write Timing Constraints : NO

Hierarchy Separator : _

Bus Delimiter : <>

Case Specifier : maintain

Slice Utilization Ratio : 100

Slice Utilization Ratio Delta : 5

---- Other Options

lso : el310_top.lso

Read Cores : YES

cross_clock_analysis : NO

verilog2001 : YES

Optimize Instantiated Primitives : NO

==========

==========

* HDL Compilation *

==========

Compiling source file "../s12/el310_blockram.v"

Module <el310_top> compiled

No errors in compilation

Analysis of file <el310_top.prj> succeeded.

==========

* HDL Analysis *

==========

Analyzing top module <el310_top>.

```
Module <el310_top> is correct for synthesis.


    Set property "resynthesize = true" for unit <el310_top>.
Analyzing module <RAMB16_S1>.
Analyzing module <vga_controller_640_60>.
Module <vga_controller_640_60> is correct for synthesis.
 =========================================================================
*                     HDL Synthesis                       *
=========================================================================
Synthesizing Unit <vga_controller_640_60>.
    Related source file is ../vga_controller_640_60.v.
    Found 11-bit up counter for signal <vcount>.
    Found 1-bit register for signal <HS>.
    Found 11-bit up counter for signal <hcount>.
    Found 1-bit register for signal <VS>.
    Found 1-bit register for signal <blank>.
    Found 11-bit comparator less for signal <$n0011> created at line 122.
    Found 11-bit comparator less for signal <$n0012> created at line 122.
    Found 11-bit comparator greatequal for signal <$n0013> created at line 114.
    Found 11-bit comparator less for signal <$n0014> created at line 114.
    Found 11-bit comparator greatequal for signal <$n0015> created at line 116.
    Found 11-bit comparator less for signal <$n0016> created at line 116.
    Found 1-bit register for signal <clk_25>.
    Summary:
        inferred   2 Counter(s).
        inferred   4 D-type flip-flop(s).
        inferred   6 Comparator(s).
Unit <vga_controller_640_60> synthesized.


Synthesizing Unit <el310_top>.
    Related source file is ../s12/el310_blockram.v.
WARNING:Xst:1780 - Signal <M22> is never used or assigned.
```

WARNING:Xst:646 - Signal <out3<9>> is assigned but never used.

WARNING:Xst:646 - Signal <out4<9>> is assigned but never used.

Found finite state machine <FSM_0> for signal <state>.

```
-----------------------------------------------------------------------
| States             | 13                                   |
| Transitions        | 16                                   |
| Inputs             | 3                                    |
| Outputs            | 13                                   |
| Clock              | clk (rising_edge)                    |
| Clock enable       | start (positive)                     |
| Reset              | rst (positive)                       |
| Reset type         | asynchronous                         |
| Reset State        | 0000000000001                        |
| Encoding           | automatic                            |
| Implementation     | LUT                                  |
-----------------------------------------------------------------------
```

Found 32-bit adder for signal <$n0003> created at line 262.

Found 32-bit adder for signal <$n0008> created at line 271.

Found 7-bit comparator less for signal <$n0011> created at line 204.

Found 7-bit comparator greatequal for signal <$n0064> created at line 204.

Found 11-bit comparator less for signal <$n0065> created at line 90.

Found 11-bit comparator less for signal <$n0066> created at line 90.

Found 7-bit adder for signal <$n0074> created at line 206.

Found 7-bit adder for signal <$n0075> created at line 207.

Found 7-bit adder for signal <$n0076> created at line 208.

Found 9-bit adder for signal <$n0077> created at line 187.

Found 9-bit adder for signal <$n0078> created at line 191.

Found 7-bit comparator greater for signal <$n0079> created at line 62.

Found 7-bit comparator less for signal <$n0080> created at line 62.

Found 7-bit comparator greater for signal <$n0081> created at line 62.

Found 7-bit comparator less for signal <$n0082> created at line 62.

Found 7-bit comparator greater for signal <$n0083> created at line 68.

Found 7-bit comparator less for signal <$n0084> created at line 68.

Found 7-bit comparator greater for signal <$n0085> created at line 64.

Found 7-bit comparator less for signal <$n0086> created at line 64.

Found 7-bit comparator greater for signal <$n0087> created at line 64.

Found 7-bit comparator less for signal <$n0088> created at line 64.

Found 7-bit comparator greater for signal <$n0089> created at line 70.

Found 7-bit comparator less for signal <$n0090> created at line 70.

Found 9-bit adder carry out for signal <$n0094>.

Found 9-bit adder carry out for signal <$n0095>.

Found 9-bit adder carry out for signal <$n0096>.

Found 9-bit adder carry out for signal <$n0097>.

Found 9-bit register for signal <Adder1in1>.

Found 9-bit register for signal <Adder1in2>.

Found 9-bit register for signal <Adder2in1>.

Found 9-bit register for signal <Adder2in2>.

Found 9-bit register for signal <Adder3in1>.

Found 9-bit register for signal <Adder3in2>.

Found 9-bit register for signal <Adder4in1>.

Found 9-bit register for signal <Adder4in2>.

Found 1-bit register for signal <data_in2>.

Found 7-bit up counter for signal <hcounter>.

Found 14-bit register for signal <init_addr2>.

Found 8-bit register for signal <M11>.

Found 8-bit register for signal <M12>.

Found 8-bit register for signal <M13>.

Found 8-bit register for signal <M21>.

Found 8-bit register for signal <M23>.

Found 8-bit register for signal <M31>.

Found 8-bit register for signal <M32>.

Found 8-bit register for signal <M33>.

Found 14-bit register for signal <read_addr>.

Found 1-bit register for signal <rw2>.

Found 1-bit register for signal <start>.

Found 1-bit register for signal <start2>.

Found 7-bit up counter for signal <vcounter>.

Found 7-bit register for signal <x1>.

Found 8-bit adder for signal <X11>.

Found 7-bit register for signal <x2>.

Found 7-bit register for signal <x3>.

Found 7-bit up counter for signal <y1>.

Found 7-bit up counter for signal <y2>.

Found 7-bit up counter for signal <y3>.

Found 8-bit adder for signal <Y31>.

Found 8-bit adder for signal <Y33>.

Found 29 1-bit 2-to-1 multiplexers.

Summary:

inferred 1 Finite State Machine(s).

inferred 5 Counter(s).

inferred 175 D-type flip-flop(s).

inferred 14 Adder/Subtracter(s).

inferred 16 Comparator(s).

inferred 29 Multiplexer(s).

Unit <el310_top> synthesized.

==========

* Advanced HDL Synthesis *

==========

Advanced RAM inference ...

Advanced multiplier inference ...

Advanced Registered AddSub inference ...

Selecting encoding for FSM_0 ...

Optimizing FSM <FSM_0> on signal <state> with one-hot encoding.

Dynamic shift register inference ...

==========

HDL Synthesis Report

Macro Statistics

FSMs : 1

Adders/Subtractors : 14

9-bit adder : 2

7-bit adder : 3

32-bit adder : 2

9-bit adder carry out : 4

8-bit adder : 3

Counters : 7

11-bit up counter : 2

7-bit up counter : 5

Registers : 42

8-bit register : 8

7-bit register : 3

9-bit register : 8

14-bit register : 2

1-bit register : 21

Comparators : 22

7-bit comparator less : 7

7-bit comparator greater : 6

11-bit comparator less : 6

7-bit comparator greatequal : 1

11-bit comparator greatequal : 2

Multiplexers : 3

1-bit 2-to-1 multiplexer : 1

14-bit 2-to-1 multiplexer : 2

===

===

* Low Level Synthesis *

===

WARNING:Xst:1710 - FF/Latch <Adder3in1_8> (without init value) is constant in block <el310_top>.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <Adder4in2_8> (without init value) is constant in block <el310_top>.

Optimizing unit <el310_top> ...

Optimizing unit <vga_controller_640_60> ...

Loading device for application Xst from file '3s200.nph' in environment C:/Xilinx.

Mapping all equations...

Building and optimizing final netlist ...

Register M11_7 equivalent to M11_3 has been removed

Register M11_6 equivalent to M11_3 has been removed

Register M11_5 equivalent to M11_3 has been removed

Register M11_4 equivalent to M11_3 has been removed

Register M21_7 equivalent to M21_4 has been removed

Register M21_6 equivalent to M21_4 has been removed

Register M21_5 equivalent to M21_4 has been removed

Register M11_2 equivalent to M11_1 has been removed

Register M11_3 equivalent to M11_1 has been removed

Register M11_1 equivalent to M11_0 has been removed

Register M21_4 equivalent to M21_3 has been removed

Register M13_7 equivalent to M13_0 has been removed

Register M13_1 equivalent to M13_0 has been removed

Register M13_2 equivalent to M13_0 has been removed

Register M13_3 equivalent to M13_0 has been removed

Register M13_4 equivalent to M13_0 has been removed

Register M13_5 equivalent to M13_0 has been removed

Register M13_6 equivalent to M13_0 has been removed

Register M12_7 equivalent to M12_6 has been removed

Register M21_3 equivalent to M21_2 has been removed

Register M12_1 equivalent to M12_0 has been removed

Register M12_2 equivalent to M12_0 has been removed

Register M12_3 equivalent to M12_0 has been removed

Register M12_4 equivalent to M12_0 has been removed

Register M12_5 equivalent to M12_0 has been removed

Register M12_6 equivalent to M12_0 has been removed

Register M33_7 equivalent to M33_0 has been removed

Register M33_1 equivalent to M33_0 has been removed

Register M33_2 equivalent to M33_0 has been removed

Register M33_3 equivalent to M33_0 has been removed

Register M33_4 equivalent to M33_0 has been removed

Register M33_5 equivalent to M33_0 has been removed

Register M33_6 equivalent to M33_0 has been removed

Register M32_7 equivalent to M32_0 has been removed

Register M32_1 equivalent to M32_0 has been removed

Register M32_2 equivalent to M32_0 has been removed

Register M32_3 equivalent to M32_0 has been removed

Register M32_4 equivalent to M32_0 has been removed

Register M32_5 equivalent to M32_0 has been removed

Register M32_6 equivalent to M32_0 has been removed

Register M31_7 equivalent to M31_0 has been removed

Register M31_1 equivalent to M31_0 has been removed

Register M31_2 equivalent to M31_0 has been removed

Register M31_3 equivalent to M31_0 has been removed

Register M31_4 equivalent to M31_0 has been removed

Register M31_5 equivalent to M31_0 has been removed

Register M31_6 equivalent to M31_0 has been removed

Register M23_7 equivalent to M23_0 has been removed

Register M23_1 equivalent to M23_0 has been removed

Register M23_2 equivalent to M23_0 has been removed

Register M23_3 equivalent to M23_0 has been removed

Register M23_4 equivalent to M23_0 has been removed

Register M23_5 equivalent to M23_0 has been removed

Register M23_6 equivalent to M23_0 has been removed

Register M21_1 equivalent to M21_0 has been removed

Register M21_2 equivalent to M21_0 has been removed

Found area constraint ratio of 100 (+ 5) on block el310_top, actual ratio is 17.

FlipFlop state_FFd2 has been replicated 1 time(s)

FlipFlop state_FFd3 has been replicated 1 time(s)

FlipFlop state_FFd4 has been replicated 4 time(s)

FlipFlop state_FFd5 has been replicated 4 time(s)

==========

* Final Report *

==========

Final Results

RTL Top Level Output File Name : el310_top.ngr

Top Level Output File Name : el310_top

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

IOs : 7

Macro Statistics :

Registers : 46

1-bit register : 22

14-bit register : 2

7-bit register : 6

8-bit register : 8

9-bit register : 8

Counters : 2

11-bit up counter : 2

Multiplexers : 3

2-to-1 multiplexer : 3

Adders/Subtractors : 19

32-bit adder : 2

7-bit adder : 8

```
#      8-bit adder                : 3
#      9-bit adder                : 2
#      9-bit adder carry out      : 4
# Comparators                     : 22
#      11-bit comparator greatequal: 2
#      11-bit comparator less     : 6
#      7-bit comparator greatequal : 1
#      7-bit comparator greater   : 6
#      7-bit comparator less      : 7

Cell Usage :
# BELS                           : 824
#      GND                       : 1
#      LUT1                      : 76
#      LUT1_L                    : 36
#      LUT2                      : 41
#      LUT2_D                    : 3
#      LUT2_L                    : 24
#      LUT3                      : 61
#      LUT3_D                    : 2
#      LUT3_L                    : 12
#      LUT4                      : 192
#      LUT4_D                    : 5
#      LUT4_L                    : 57
#      MUXCY                     : 155
#      MUXF5                     : 5
#      VCC                       : 1
#      XORCY                     : 153
# FlipFlops/Latches              : 215
#      FDC                       : 4
#      FDCE                      : 75
#      FDCPE                     : 22
#      FDE                       : 107
```

```
#      FDPE                : 5
#      FDRE                : 1
#      FDSE                : 1
# RAMS                     : 2
#      RAMB16_S1           : 2
# Clock Buffers            : 1
#      BUFGP               : 1
# IO Buffers               : 6
#      IBUF                : 1
#      OBUF                : 5
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s200ft256-4

 Number of Slices:              296  out of   1920    15%
 Number of Slice Flip Flops:    215  out of   3840     5%
 Number of 4 input LUTs:        509  out of   3840    13%
 Number of bonded IOBs:           6  out of    173     3%
 Number of BRAMs:                 2  out of     12    16%
 Number of GCLKs:                 1  out of      8    12%


=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
```

```
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 192   |
vga_cont_clk_25:Q                  | NONE                   | 25    |
-----------------------------------+------------------------+-------+

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 7.214ns (Maximum Frequency: 138.619MHz)
   Minimum input arrival time before clock: 5.862ns
   Maximum output required time after clock: 11.294ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

--------------------------------------------------------------------------------
Timing constraint: Default period analysis for Clock 'clk'
Delay:               7.214ns (Levels of Logic = 13)
  Source:            Adder2in2_0 (FF)
  Destination:       Adder1in2_8 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: Adder2in2_0 to Adder1in2_8
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
```

```
    FDE:C->Q              4   0.720   0.629  Adder2in2_0 (Adder2in2_0)
    LUT2_D:I0->LO         1   0.551   0.000  Madd__n0096_inst_lut2_81 (N19410)
    MUXCY:S->O            1   0.500   0.000  Madd__n0096_inst_cy_8 (Madd__n0096_inst_cy_8)
    MUXCY:CI->O           1   0.064   0.000  Madd__n0096_inst_cy_9 (Madd__n0096_inst_cy_9)
    MUXCY:CI->O           1   0.064   0.000  Madd__n0096_inst_cy_10 (Madd__n0096_inst_cy_10)
    MUXCY:CI->O           1   0.064   0.000  Madd__n0096_inst_cy_11 (Madd__n0096_inst_cy_11)
    MUXCY:CI->O           1   0.064   0.000  Madd__n0096_inst_cy_12 (Madd__n0096_inst_cy_12)
    MUXCY:CI->O           1   0.064   0.000  Madd__n0096_inst_cy_13 (Madd__n0096_inst_cy_13)
    MUXCY:CI->O           1   0.064   0.000  Madd__n0096_inst_cy_14 (Madd__n0096_inst_cy_14)
    XORCY:CI->O           3   0.904   0.577  Madd__n0096_inst_sum_15 (out2<7>)
    LUT1_L:I0->LO         1   0.551   0.000  _n0001<7>1 (_n0001<7>)
    MUXCY:S->O            0   0.500   0.000  Madd__n0078_inst_cy_63 (Madd__n0078_inst_cy_63)
    XORCY:CI->O           1   0.904   0.240  Madd__n0078_inst_sum_64 (_n0078<8>)
    LUT4_L:I1->LO         1   0.551   0.000  _n0054<8>16 (_n0054<8>)
    FDE:D                 0.203          Adder1in2_8
    ----------------------------------------
    Total                 7.214ns (5.768ns logic, 1.446ns route)
                              (80.0% logic, 20.0% route)

--------------------------------------------------------------------------------
Timing constraint: Default period analysis for Clock 'vga_cont_clk_25:Q'
Delay:               7.003ns (Levels of Logic = 15)
  Source:            vga_cont_hcount_15 (FF)
  Destination:       vga_cont_vcount_10 (FF)
  Source Clock:      vga_cont_clk_25:Q rising
  Destination Clock: vga_cont_clk_25:Q rising

  Data Path: vga_cont_hcount_15 to vga_cont_vcount_10
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
    FDCPE:C->Q            6   0.720   0.688  vga_cont_hcount_15 (vga_cont_hcount_15)
    LUT4:I0->O            4   0.551   0.629  vga_cont__n000310 (CHOICE932)
```

```
    LUT3_D:I0->O         18   0.551   1.066  vga_cont__n000343 (vga_cont__n0003)
    LUT3_L:I0->LO         1   0.551   0.000  vga_cont__n000055 (vga_cont__n0000)
    MUXCY:S->O            1   0.500   0.000  vga_cont_vcount_inst_cy_65 (vga_cont_vcount_inst_cy_65)
    MUXCY:CI->O           1   0.064   0.000  vga_cont_vcount_inst_cy_66 (vga_cont_vcount_inst_cy_66)
    MUXCY:CI->O           1   0.064   0.000  vga_cont_vcount_inst_cy_67 (vga_cont_vcount_inst_cy_67)
    MUXCY:CI->O           1   0.064   0.000  vga_cont_vcount_inst_cy_68 (vga_cont_vcount_inst_cy_68)
    MUXCY:CI->O           1   0.064   0.000  vga_cont_vcount_inst_cy_69 (vga_cont_vcount_inst_cy_69)
    MUXCY:CI->O           1   0.064   0.000  vga_cont_vcount_inst_cy_70 (vga_cont_vcount_inst_cy_70)
    MUXCY:CI->O           1   0.064   0.000  vga_cont_vcount_inst_cy_71 (vga_cont_vcount_inst_cy_71)
    MUXCY:CI->O           1   0.064   0.000  vga_cont_vcount_inst_cy_72 (vga_cont_vcount_inst_cy_72)
    MUXCY:CI->O           1   0.064   0.000  vga_cont_vcount_inst_cy_73 (vga_cont_vcount_inst_cy_73)
    MUXCY:CI->O           1   0.064   0.000  vga_cont_vcount_inst_cy_74 (vga_cont_vcount_inst_cy_74)
    MUXCY:CI->O           0   0.064   0.000  vga_cont_vcount_inst_cy_75 (vga_cont_vcount_inst_cy_75)
    XORCY:CI->O           1   0.904   0.000  vga_cont_vcount_inst_sum_75 (vga_cont_vcount_inst_sum_75)
    FDCPE:D                   0.203          vga_cont_vcount_10
    ----------------------------------------
    Total                     7.003ns (4.620ns logic, 2.383ns route)
                              (66.0% logic, 34.0% route)

--------------------------------------------------------------------------------
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
Offset:              5.862ns (Levels of Logic = 2)
  Source:            rst (PAD)
  Destination:       Adder3in2_8 (FF)
  Destination Clock: clk rising

  Data Path: rst to Adder3in2_8
                            Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
    IBUF:I->O           117   1.930   1.406  rst_IBUF (rst_IBUF)
    LUT2:I0->O           84   0.551   1.373  Ker120471 (N12049)
    FDE:CE                    0.602          Adder3in1_3
```

```
   ----------------------------------------
   Total                    5.862ns (3.083ns logic, 2.779ns route)
                               (52.6% logic, 47.4% route)

--------------------------------------------------------------------------------
Timing constraint: Default OFFSET OUT AFTER for Clock 'vga_cont_clk_25:Q'
Offset:              11.294ns (Levels of Logic = 7)
  Source:            vga_cont_hcount_19 (FF)
  Destination:       B (PAD)
  Source Clock:      vga_cont_clk_25:Q rising

  Data Path: vga_cont_hcount_19 to B
                            Gate     Net
   Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
   ----------------------------------------  ------------
    FDCPE:C->Q           5   0.720   0.658  vga_cont_hcount_19 (vga_cont_hcount_19)
    LUT4:I0->O           4   0.551   0.629  Ker120611 (N12063)
    LUT4:I3->O           1   0.551   0.000  _n0111132_F (N19298)
    MUXF5:I0->O          1   0.360   0.240  _n0111132 (CHOICE236)
    LUT4:I3->O           1   0.551   0.240  _n0111146 (_n0111)
    LUT4:I0->O           1   0.551   0.240  pixel_out17 (CHOICE193)
    LUT2:I1->O           3   0.551   0.577  pixel_out21 (R_OBUF)
    OBUF:I->O                4.875          G_OBUF (G)
   ----------------------------------------
   Total                   11.294ns (8.710ns logic, 2.584ns route)
                               (77.1% logic, 22.9% route)

--------------------------------------------------------------------------------
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
Offset:              9.953ns (Levels of Logic = 3)
  Source:            ram (RAM)
  Destination:       B (PAD)
  Source Clock:      clk rising
```

Data Path: ram to B

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
RAMB16_S1:CLK->DO0	9	2.382	0.777	ram (data_out)
LUT4:I1->O	1	0.551	0.240	pixel_out17 (CHOICE193)
LUT2:I1->O	3	0.551	0.577	pixel_out21 (R_OBUF)
OBUF:I->O		4.875		G_OBUF (G)
Total		9.953ns (8.359ns logic, 1.594ns route)		
		(84.0% logic, 16.0% route)		

==========

CPU : 19.41 / 23.39 s | Elapsed : 19.00 / 21.00 s

-->

Total memory usage is 74244 kilobytes