DAT175:

Topics in Electronic System Design

Analog Readout Circuitry for Hearing Aid in STM90nm

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1. Introduction

In this project, the aim is to design an adjustable gain pre-amplifier for a hearing aid circuitry. ST Microelectronics 90nm CMOS process was used for the application. Due to the fundamental limit on power supply, circuits operating in lower inversion levels were investigated. Two main solutions, one with continuous time and one with discrete time are presented.

2. Technology Comparison

Before starting the design, the chosen technology is compared to a better-known technology, which is AMS 0.35µ CMOS within a case study. Two folded-cascode amplifiers are designed with the same specifications on bandwidth, slew-rate, load and overdrive voltage. The results of the comparison can be observed in Table 1.

AMS 0.35u	STM 90nm
more area	less area
more gain	less gain
voltage swing around 2V	voltage swing less than 0.1V
supply voltage 3.3V	supply voltage 1V

Table 1: Comparison between AMS 0.35u and STM 0.09u

As Table 1 suggests the main problem with the 90nm process was the voltage swing. Since, the pre-amplifier is the first circuitry the limit on the voltage swing will limit the overall performance of the system such that the analog-to-digital converter needs to be very precise, if not the effective number of bits will limit the performance of the digital part.

3. Possible Implementation Methods

Of the available solutions to increase the voltage swing, operating transistors in weak inversion is chosen. The main idea is applying a lower overdrive voltage, which decreases the minimum amount of drain-to-source voltage required for putting a transistor into saturation. As the gate-to-source, voltage is decreased from the values above the threshold to under the threshold, the inversion level of the transistor decreases and the drain current of a MOS device becomes dominated by the diffusion current, which is proportional to exponential of overdrive voltage.

The overdrive voltage (Vov), which is the excess voltage applied to gate after the threshold voltage is reached, is mainly negative at weak inversion, meaning that the transistors are conducting below threshold voltage. In standard analog circuit design, the square law is used for calculating the drain current or aspect ratios. However, square law is valid in certain limits which are $Vgs > Vth$ and $Vds < Vov$. Thus, square law is not sufficient for designing in weak inversion. Instead, EKV model is used as it offers a continuous and accurate modelling of the drain current as the gate-to-source voltage changes. The model is developed by C. C. Enz, F. Krummenacher and E. A. Vittoz; it is aimed for exploiting the sub-threshold current for circuit design [1]. In addition to extra constants based on the process, the equations also include an extra design variable, which is the inversion coefficient. Inversion coefficient introduces low power and transistors that are more efficient in a different way than square law.

At weak inversion, the necessary drain-to-source voltage to put the transistor into saturation decreases to $4 \times kt/q$,where $k$is the Boltzmann constant with the value of $1.380\,6504 \times 10^{-23}\,JK^{-1}$, t is temperature with $300K$in room conditions and q is the unit charge of $1.602 \times 10^{-19}\,C$. These values under room conditions make up 103.6mV [2]. In addition, it must be noted that this fundamental limit is independent of process and only depends on the temperature of operation.

Reduced drain-to-source voltage allows higher voltage swing. Yet, the main drawbacks of operation in weak inversion can be summarized as follows. Compared to strong inversion, the lower overdrive voltage forces the transistor to have a larger aspect ratio in order to produce same amount of current. Thus, to keep the sizes of the transistors respectable, the circuits are designed for lower amounts of bias current, and this limits the speed and frequency response. However, it is a viable solution in designing hearing aid since a slow but very low power circuit is necessary. The advantages and disadvantages of using different levels of inversion can be summarized with the following table.

Weak Inversion (Vov<-72mV or IC<0.1)	Moderate Inversion (-72mV <Vov<225mV or 0.1<IC<10)	Strong Inversion (225mV<Vov or 10<IC)
Large aspect ratios Small bandwidth High gm/Id High leakage	Moderate aspect ratios Moderate bandwidth Moderate gm/Id Little velocity saturation	Small aspect ratios Wide bandwidth Low gm/Id Current drop due to velocity saturation

Table 2: Comparison between Weak, Moderate and Strong Inversion

4. Design Flow

The design approach can be simplified as follows:

- Extract specifications
- Choose circuit topology according to specifications
- Calculate the bias currents
- Decide on the inversion level through either IC or Vov

- Choose transistor length according to the specifications and calculate width

Normalized inversion coefficient (IC) is:

$$IC = \frac{I_D}{I_o \times \frac{W}{L}}$$

Where I_o is defined as the technology current:

$$I_o = 2 \times n_0 \times \mu_o \times C'_{ox} \times U_T^2$$

Even though the design flow is trivial, the generally known equations of square law are not applicable in weak inversion. EKV model [1] is used in calculating the properties of transistors in weak inversion [2].

$$I_D(\text{WI}) = 2 \times \text{n} \times \mu \times \text{C}'_{ox} \times U_T^2 \times \left(\frac{W}{L}\right) \times ln^2\left(1 + e^{\frac{V_{GS}-V_T}{2 \times n \times U_T}}\right)$$

In weak inversion, the current equation simplifies to the following equation [3].

$$I_D(\text{WI}) = 2 \times \text{n} \times \mu \times \text{C}'_{ox} \times U_T^2 \times \left(\frac{W}{L}\right) \times \left(e^{\frac{V_{GS}-V_T}{n \times U_T}}\right)$$

$$\text{Where } n = 1 + \frac{C'_{DEP}}{C'_{ox}},\ U_T = \frac{kt}{q}$$

In addition, the transconductance is:

$$gm(\text{WI}) = \frac{I_D}{n \times U_T}$$

Here n is the substrate factor. It introduces the effect of substrate to drain current. In weak inversion, it is also called the weak inversion slope factor. Since it is inversely proportional to inversion, it is assumed as 1 square law strong inversion drain current formula. On the other hand, it has an approximate value of 1.4 in weak inversion. n_0 is defined as the value of n in average moderate inversion [2].

5. Circuits and Results

After an initial literary search, Kim et al. [4**]** has been decided as the main reference paper. Final performance expectations are extracted from various papers. For the specifications of individual sub-blocks system level simulations and hand calculations were done.

Two types of pre-amplifiers have been designed. The first circuit operates in continuous time domain while the second one operates in discrete time domain. Unfortunately, both circuits suffer from certain drawbacks, which are explained below.

5.a Continuous Time Circuits

The most apparent advantage of continuous time circuits are, they do not include clocks. Thus, they do not suffer distortions caused by clocks, clock feed-through. Moreover, the power and area spent for the clocks are avoided.

5.a.1 Overall Circuitry

The mechanism of the pre-amplifier can be explained with Figure 1. The input while entering the op-amp also goes through the peak detector and the comparator. The output of the comparator controls the voltage applied to the gate of the transistors used as resistive feedback. This operation enables one-knee multiple-gain, where the input is below the threshold gain is higher than the gain when the input is above the threshold. The aim in not using a constant gain amplifier is protecting the ear system from the high amplitude sounds.

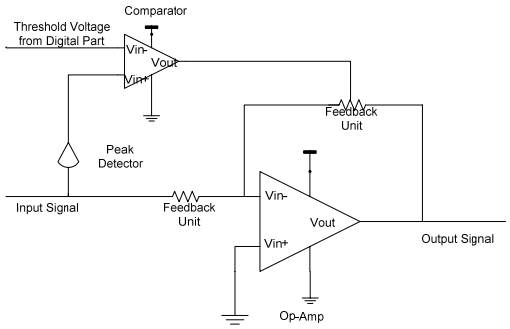

Figure 1: Architectural View of the Pre-Amplifier

5.a.2 Op-amp and Common-Mode Feedback

A two-stage operational amplifier topology is chosen as the heart of the pre-amplifier circuitry. The topology and the common-mode feedback circuitry can be observed in Figure 2 and Figure 3. The aim behind choosing the two-stage topology is maximizing the voltage swing. The idea behind the two-stage topology is, in the first stage the gain is provided while in the second stage the number of transistors between the ground and the vdd is kept at minimum to provide a larger voltage swing. The first stage can be cascaded in order to increase the gain.

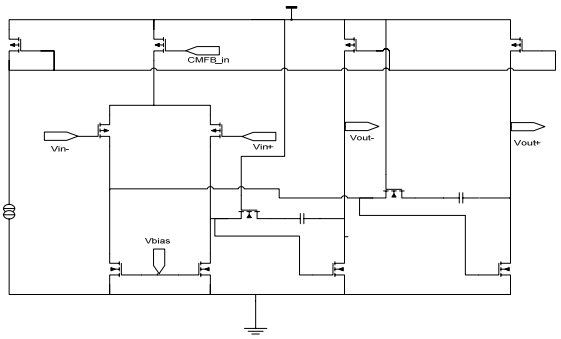

Figure 2: Schematic of Two-Stage Op-amp

The common-mode feedback circuitry is a necessity in order to keep the circuitry at the right dc points when fully differential circuits are used, if not used the outputs stick to vdd or to ground. One drawback of the two-stage topology is it requires adjustments in its transfer function to have good phase response. This is done by putting a serial RC feedback between two stages, which corresponds to inserting a zero in the transfer function that has a value equal to the non-dominant pole. 70° degree is the desired value for phase margin, as it prevents settling problems such as overshoot and ringing that occur due to bad phase response.

The resistor based CMFB circuits are known for limiting the voltage [5], while the resistive load limits the gain or a large resistance needs to be used. To avoid these, a transistor based CMFB circuit is used [6].

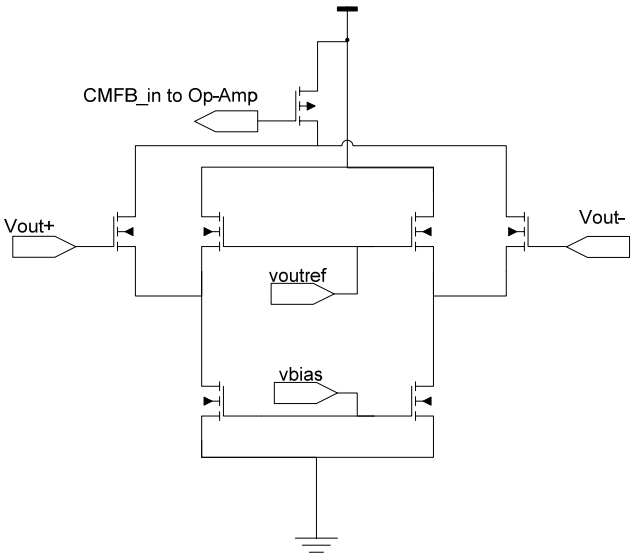

Figure 3: Schematic of CMFB for Two-Stage Op-amp

5.a.3 Comparator

In continuous time, the comparator can be implemented as a single-ended op-amp, which would have the value to compare as the positive input and the threshold value as the negative input. The positive output then will go to ground if the input is smaller than the threshold and vice versa. Due to the difference in application, the op-amp used in the pre-amplifier part should not be used. Here, the settling speed, power and the input offset are important parameters while the accuracy of the gain or the absolute value of the gain are not. Thus, the op-amp must be optimized for these parameters.

5.a.4 Results

With single-ended circuits, a voltage swing of 700mV without gain degradation has been reached initially. However, this value dropped significantly with the addition of the CMFB to a differential value of 500mV. The achieved gain was controllable via the transistors in the feedback path up to 62dB.

5.b Clocked Circuits

Since the linearity limited by the CMFB circuitry could not be increased further, clocked circuits are chosen as an alternative for following reasons. With the clocked circuitry the op-amp and the CMFB will work in different phases, thus the output swing and the linearity will be less affected by the CMFB. However, adding clocks will introduce disturbances in the signals and using switches and capacitances will introduce extra noise, circuitry and area to the design. Yet, eventually clocks were necessary in continuous version in order to implement a peak detector.

5.b.1 Overall Circuitry

The general algorithm of the circuitry is same as the continuous case. Yet, resistive circuits are replaced with switched-capacitor circuits. CMOS switches put in the signal path to control the data flow and enabling sample and hold operations as. Even though, the clocked gain block in Figure 4 can perform the sample-and-hold operation [7], an extra sample-and-hold circuit has been put before the pre-amplifier to increase the stability and control.

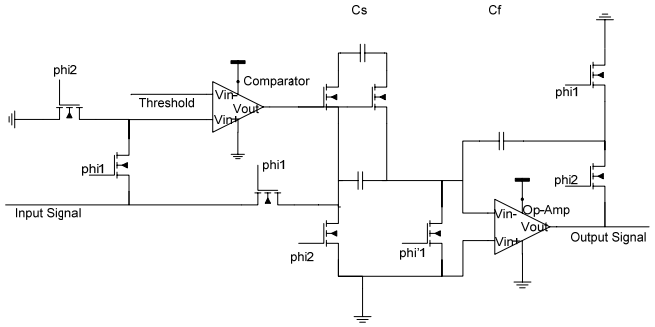

Figure 4: Discrete Time Gain Block

5.b.2 Op-amp and CMFB

Folded-cascode topology is used as the op-amp, since it has been investigated more. Folded-cascode topology provides less output swing, but it was planned to be replaced with two-stage op-amp once the system started to operate as desired. The folded-cascode structure can be observed in Figure 5. The CMFB circuit shown in Figure 6 is in fact a combination of switches and capacitances where the difference between two capacitances, one with initially charged to the desired output node voltage and one charged to the output node voltage is feedback to the op-amp to correct the output node [8]. This restoration operation is done in one phase, while the amplification operation is done in a separate phase.

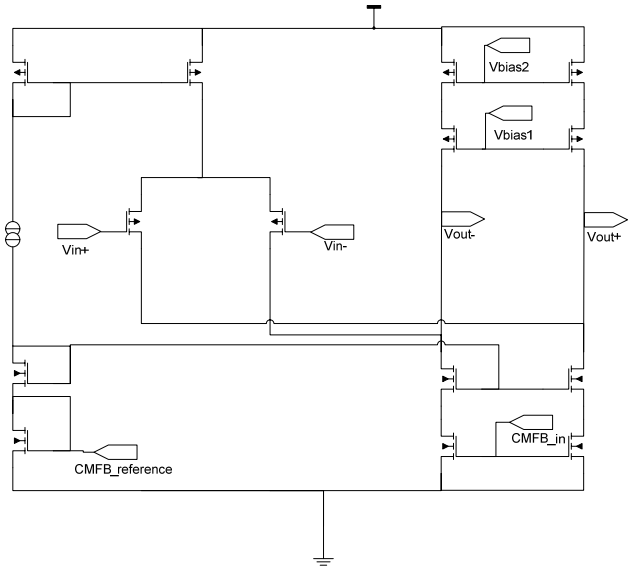

Figure 5: Schematic of Folded-Cascode Op-amp

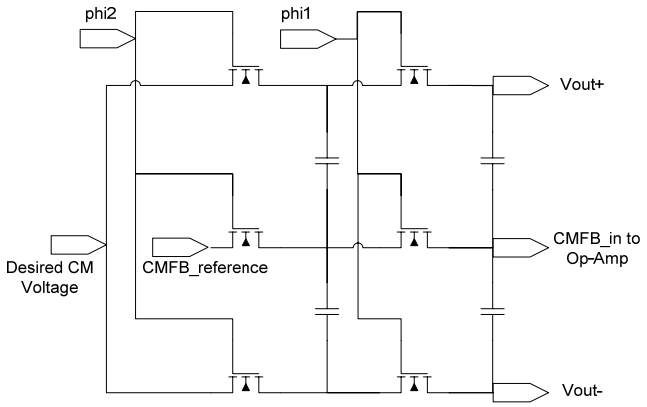

Figure 6: Schematic of CMFB for Folded-Cascode Op-amp

5.b.3 Comparator

In discrete time, the comparator can be realized with combination of an amplifier and a latch circuitry. Yet, in this design the comparator used in continuous time is used such that in the off-state when the sample and hold circuitry is restoring itself, ground is applied as the input so that the default state of the system is the high-gain stage.

5.b.4 Results

The sample and hold circuitry has been set to work correctly. However, the gain circuit had problems with settling. The reason was that the load capacitances introduced by the CMFB circuit was large. There are three ways to solve this problem. The first one is decreasing the clock frequency, in order to provide the op-amp with more time for settling yet the clock frequency was already at 20KHz, which means it can sample at most signals with a frequency of 10KHz. Another way is increasing the bias current to increase the op-amp speed; however, this was also not a viable option since the aspect ratio of the transistors become unrealistic as they operate in weak inversion. The last option is decreasing the value of the load capacitance. In fact, the capacitances should be set to the minimum value that gives tolerable kt/C noise, however they had to be set to larger values due to leakage current. When the CMFB capacitances are chosen as 1pF, a voltage change of 58.6mV was measured in 25µs, which results in a current of 2.34nA. The current has been traced to the gates of the devices connected to the capacitor. The observed gate current was 2.44nA. The preliminary performance metrics of the circuit with 10pF CMFB capacitors in comparison with the reference work [9] can be found in Table 3. It must be noted that even though the leakage was negligible, the circuit was unable to settle at the given time and the area and the power was dominated by the capacitances.

	This Work	Reference Work
Power	186uW	32uW
Area	0.019mm^2	0.057mm^2
Supply Voltage	1V	0.9V

Table 3: Comparison between the reference pre-amplifier and the work presented in this report

6. Conclusions

The scaling of CMOS does not help very much on the analog side, and the main reason is the scaling of the supply voltage. However, with the increase in the zero current gain frequency, operation in weak inversion becomes a viable option. On the other side, leakage is an important problem, thus, operation in moderate inversion may be a better choice as it is a compromise between strong inversion and weak inversion. Yet, one problem here might be the reliability of the models.

Using the inversion coefficient is a very powerful design strategy, as it gives another dimension, which the designer can control. As the inversion coefficient is lowered, it enables the low power design since the required supply voltage for a given circuitry is decreased. However, speed is reduced as the cost.

As a conclusion lower inversion levels seems as a good choice when the required circuitry needs to have low supply voltage, low power dissipation, low speed and low bandwidth. Thus, one main application area is the circuits for biomedical purposes and another main application is electronic watches.

For this application, the STM 90nm process has been unfruitful, yet the alternative cannot be the AMS 0.35µ process discussed in part 2 of the report. Since the hearing aid includes both digital and analog parts, one should also consider the other part while choosing the process. Thus, the alternative process can be STM 130nm. With this choice, the aim is to enable the integration of digital and analog parts onto the same

die, while trying to optimize performance for both domains.

7. References

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